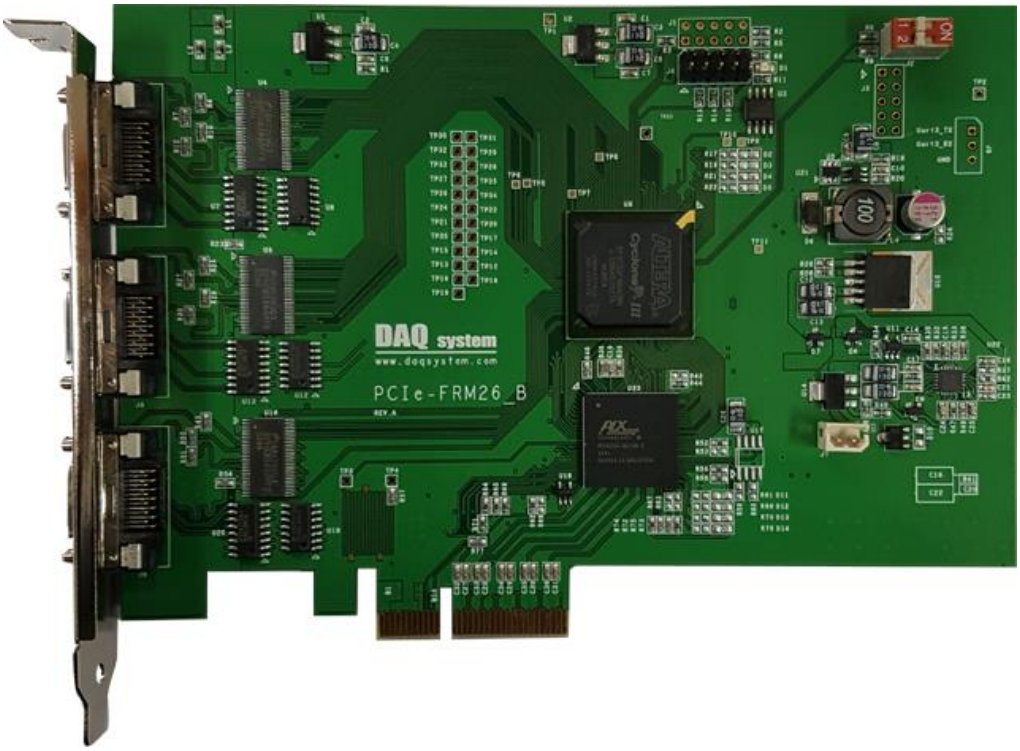
PCIe-FRM26_B

User Manual

Version 1.3



DAQ SYSTEM
Measurement & Automation

Contents

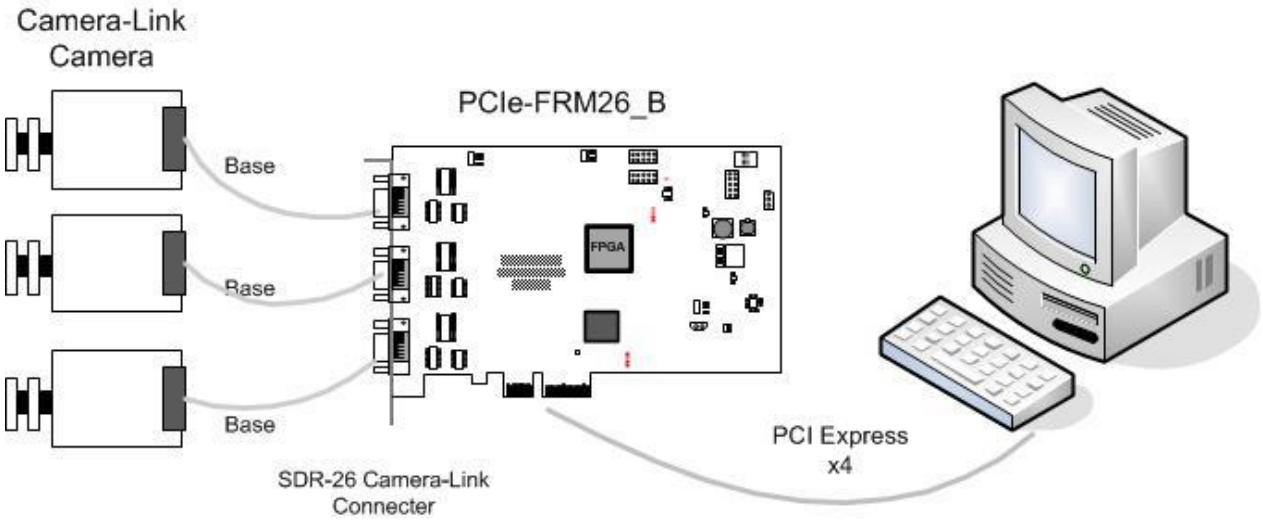
1. Introduction

PCIe-FRM26_B is an image acquisition device that supports cameras compatible with 3 Base configuration camera Links. PCIe-FRM26_B acquires images in real time and sends them to the host PC. The easy installation method and fast image transfer make it a suitable device to meet the needs of the industry with low cost and high efficiency.

The sample program provided by the DQ system is provided in the form of a source so that the API provided to use the board can be tested briefly, so the user can modify it and use it. Refer to Chapter 5 Sample Program for detailed explanation.

The SDR 26-pin connector can be connected to a Camera Link compatible camera, and channels 0 to 2 are formed from the bottom connector (J8). In addition, each SDR connector provides 4 pairs of RS-422 signal lines and 4 CC (Camera Control) signals. Refer to 3.3 Connector Pin-Out for detailed explanation.

It is a board that transmits the captured image frame to the PC through the PCI Express 4x interface method in conjunction with the standard camera. The operation of the board is controlled by the program API, and the figure below shows the interlocking operation of the board.



[Figure 1-1. PCIe-FRM26_B Board Usage]

In [Figure 1-1], PCIe-FRM26_B is installed in the PCI Express slot in the PC and receives from the camera through the Camera-Link standard interface through the image frame. It is responsible for transmitting the received data to the application program through the PCI Express 4x interface.

1-1 Product Features

Items	Description	Remark
Hardware		
PC Interface	PCI Express 4x	
Operation Power	PC Power	+3.3V (Max 1.1A) +12V (Max 1A).
Video Interface	3 Basel Camera Link	
Feature	Area Scan Camera Pixel Clock : 20 ~ 85MHz	
On-board Memory		
Communication	UART(Data bit 8, 1 start, 1 stop, No parity, 9600/19200/38400/57600 /115200bps)	
Simultaneous use of boards	Max. 4	
Software		
OS	Windows 2000/XP/7/8/10 (32/64bit)	
API	Windows Client DLL API	
Development		
Support	Sample Program	VC++
Environmental conditions		
Operating temperature range	0 ~ 60℃	
Storage temperature range	-20 ~ 80℃	
Humidity range	5 ~ 95%	Non-condensing
Board size	159.5mm X 112.5mm	PCB Board Size

1-2 Product Applications

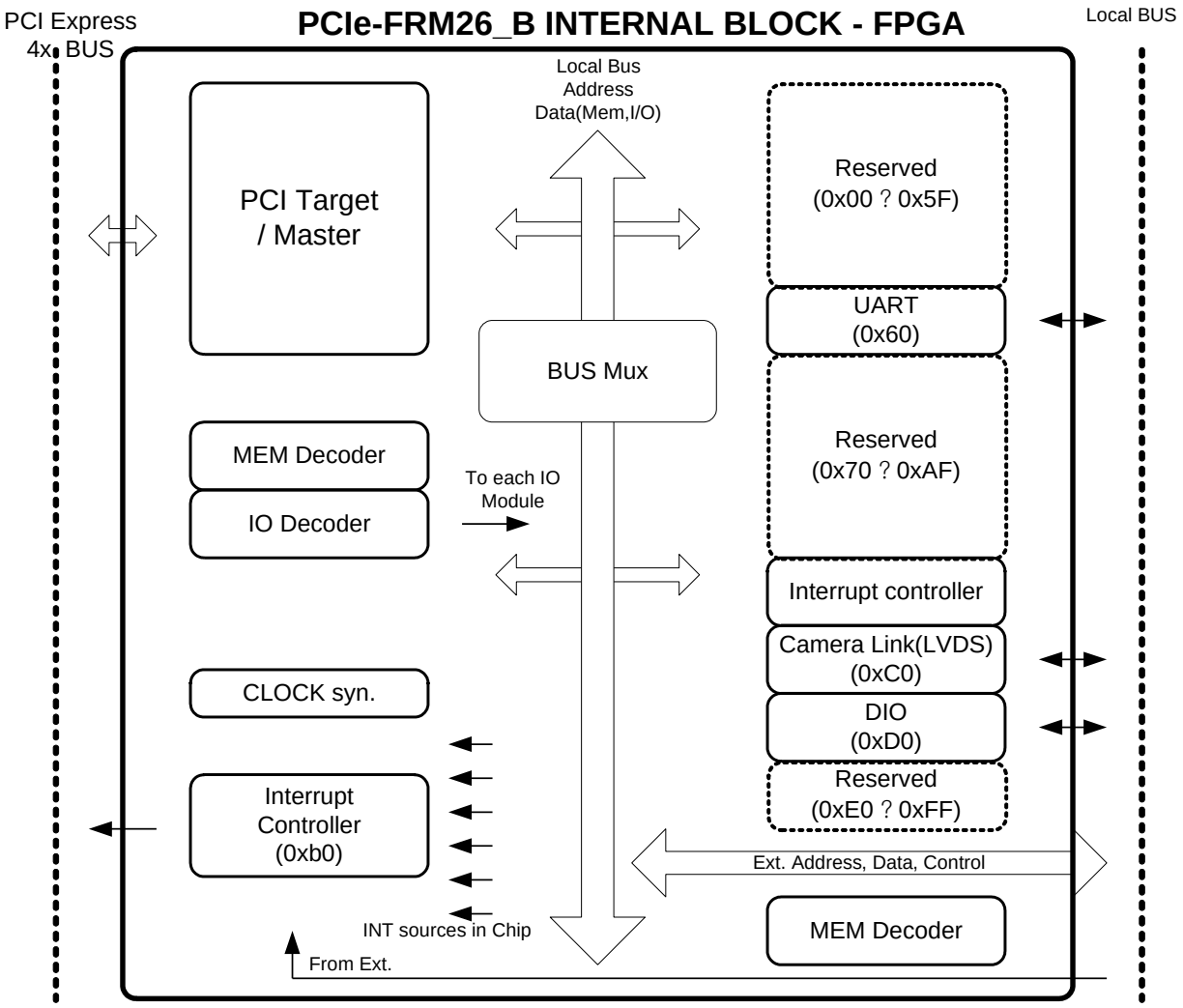
- Image recognition (Pattern, particle, etc.)
- Inspection equipment (Sensor, Semiconductor, Device etc.)
- Security Solution
- Black and White, Color Image Display
- Medical Image Capture (X-ray, Supersonic etc.)

2. PCIe-FRM26_B Board Function

2-1 Block Diagram

As shown in the figure below, in the case of PCIe-FRM26_B, FPGA Core Logic is in charge of overall control. Main functions include Frame Data reception, Camera Control signal, and UART function.

These functions are performed using API in PC through PCI Express 4x interface.



[Figure 2-1. PCIe-FRM26_B Block Diagram]]

The FPGA core logic is programmed using JTAG, and the logic program is saved in FPGA Program Logic and loaded when power is applied.

2-2 Camera Link

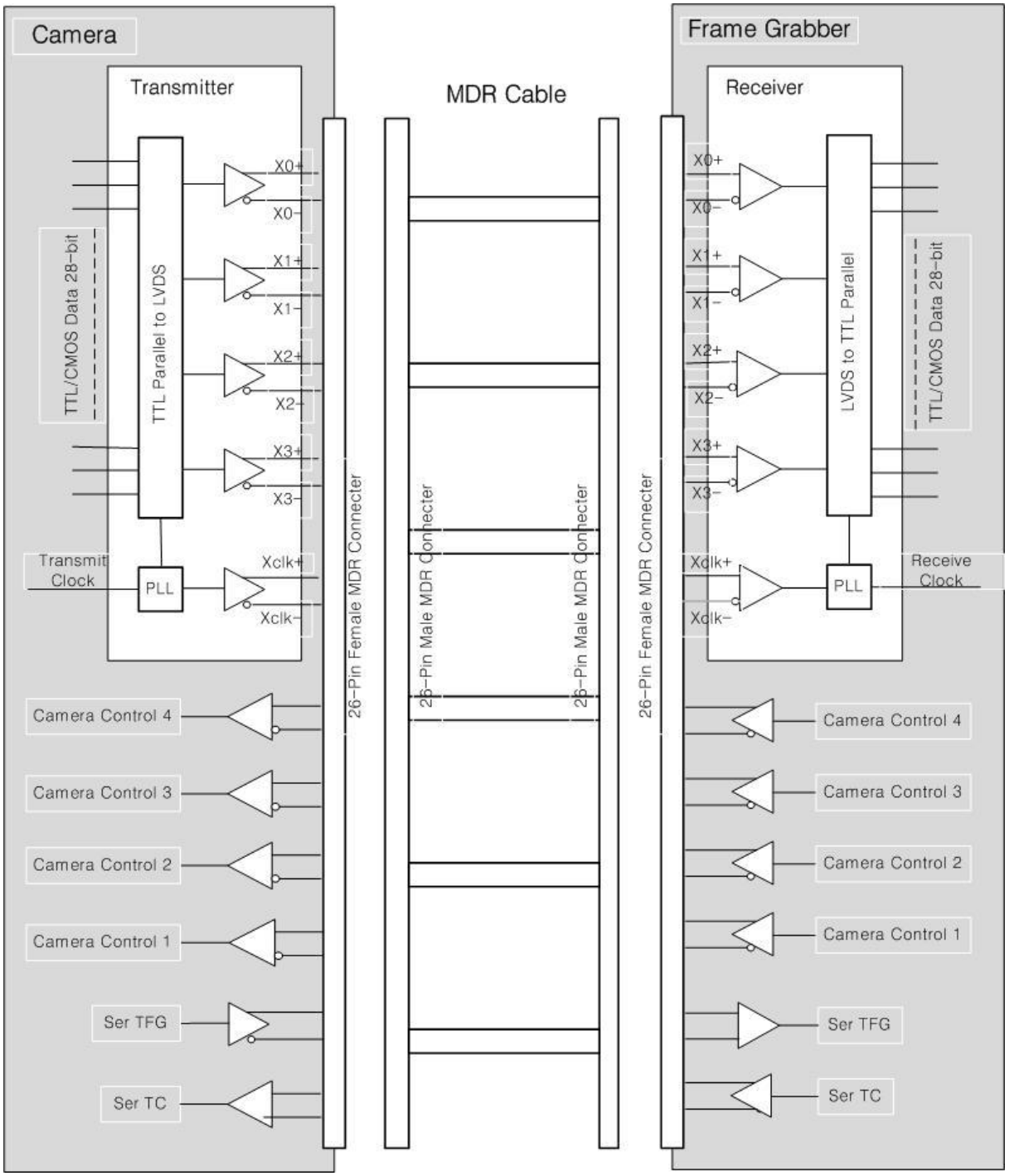
Camera Link is a communication interface developed for use in vision applications. In the past, camera manufacturers and frame grabber manufacturers used their own standard connectors and cables. This caused a lot of confusion and cost increase for users. In order to resolve this confusion, increasing data rate, and confusion in data transmission, the specifications of the Camera Link interface are the specifications of cable or connector assembly, transmission speed and It was made with regulations such as transmission method.

Many digital video solutions currently use LVDS (Low Voltage Differential Signal) communication defined by RS-644. RS-644 LVDS has become the Camera Link standard by improving the existing RS-422 method, which had inconvenient cables and limited transmission speed. LVDS can transmit data at high speed by using a differential signal with a low voltage swing. Compared to the existing single-ended signal using one line, the differential signal transmits the signal using two complementary lines. This transmission structure has the characteristics of large-scale common-phase voltage rejection, low power consumption, and excellent noise immunity, which is impossible with single-ended systems that only reference ground for data transmission.

The camera link has several configurations according to the amount of data to be transmitted. In case of Base Configuration, it is composed of 28 bits including 24-bit pixel data, Data Valid, Frame Valid Line Valid, 3-bit video sync signal line of Line Valid, and Line Valid, and one reserved signal line, and can transmit 2.04 Gbit/s (256 MB/s). Medium Configuration can transmit a 48-bit video signal at 4.08Gbit/s (510Mb/s), and Full Configuration can transmit a 64-bit video signal at 5.44Gbit/s (680MB/s). Camera Link requires two cables to carry more than the Medium specification.

The transceiver stage converts this 28/48/64 bit CMOS/TTL data into 4/8/12 LVDS data streams. The converted signal is transmitted to the MDR cable according to the Transmit Clock, and the receiver on the other side converts these 4/8/12 LVDS data into a 28/48/64 bit CMOS/TTL parallel signal according to the Receive Clock. This channel link technology is being used as a low-cost chipset that is easy to learn and portable, so that it can be used immediately.

Camera Link interface includes Base Configuration, Medium Configuration, and Full Configuration. Base Configuration uses four RS-644 LVDS pairs for transmitter/receiver and camera control as shown in [Figure 2-2], and two RS-644 LVDS pairs for communication between camera and frame grabber. . The data transmitted serially through the 26-Pin MDR Cable is changed to 28-bit parallel image data at the Receive end of the frame grabber and used.

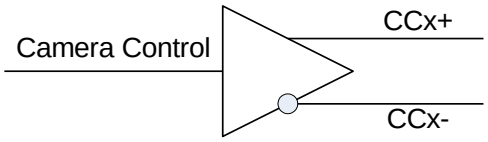


[Figure 2-2. Base Camera Link Block Diagram]

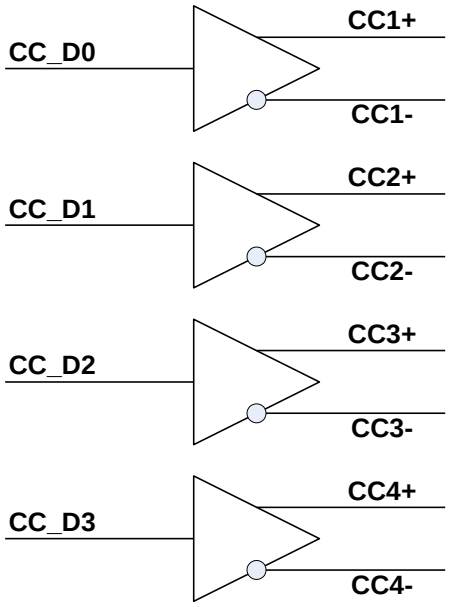
2-3 Camera Link & PCIe-FRM26_B

PCIe-FRM26_B supports Camera Link Base Configuration. Base Configuration consists of 4 LVDS signal lines serializing 28-bit parallel signals including 24 data bits and 4 enable signals Frame Valid, Line Valid, Data Valid, and a spare, and 1 LVDS signal line for synchronizing with the camera. , Asynchronous serial communication including 4 CC (Camera Control) signals and 2 LVDS lines for communicating with the camera transmits a total of 11 LVDS signal lines through one SDR cable.

The transmitted signal parallelizes 12 video LVDS serial signals into 64-bit parallel video signals and control signals for each specification (Frame Valid, Line Valid, Data Valid, and a spare) through the Channel Link chip in PCIe-FRM26_B. In addition, a clock signal is made with one LVDS to synchronize the signal between the camera and PCIe-FRM26_B, and the remaining cameras control signals and communication signals are converted into general TTL signal levels and used.

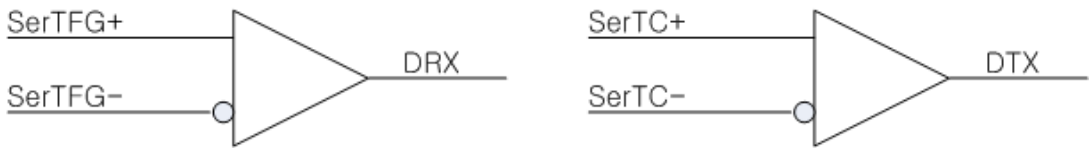


The figure shows the Camera Control output circuit that can send the control signal from the PCIe-FRM26_B board to the Camera through the Camera-link cable. A total of 4 digital outputs are output through the differential method. Each output is mapped to a digital output and becomes an output. Each bit position is shown in [Figure 2-3] below.



[Figure 2-3. Camera Control LVDS Digital Output Circuit]]

The figure below shows the circuit that uses the serial input signal input through the Camera-link cable as a general input on the PCIe-FRM24_B board.

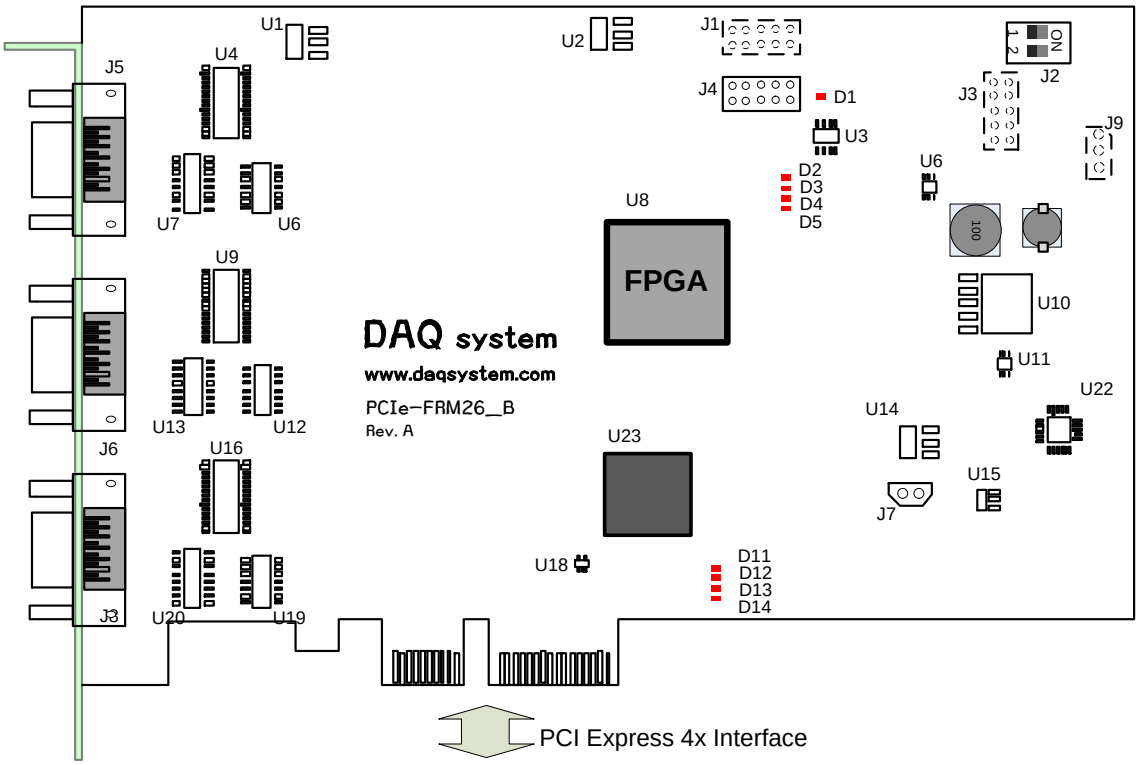


[Figure 2-4. Serial Communication LVDS Digital Output Circuit]

3. PCIe-FRM26_B Board Description

Each important board function is briefly described. For detailed function information, please refer to the parts specification.

3-1 PCIe-FRM26_B Board Layout



[Figure 3-1. PCIe-FRM26_B Layout]

There are eight LEDs on the board, and the description of each is as follows.

D1 : Lights up when the board finishes configuration and ready for operation.

D2 ~ D5 : Test purpose

D11 ~ D14 : This is the PCI Express 4 Lane Status Indicator, which lights up when Lane (0~3) is normal.

3-2 Device Features

(1) **SDR-26 Connecter : J5, J6, J8**

Camera Link Base Connector

(2) **LVDS Link : U4, U6, U7, U9, U12, U13, U16, U19, U20**

Receive an image frame.

(3) **FPGA : U8**

All of the board functions are controlled by the Logic program of the FPGA.

(4) **PCI Express Chipset : U23**

PCI Express Bridge.

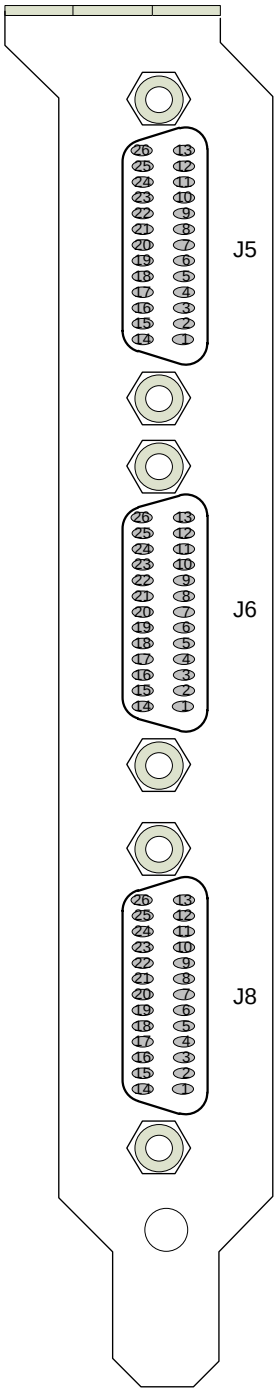
(5) **Regulator : U1, U2, U14**

It supplies the power used by the board.

3-3 Connector Pin-out

The connectors and jumpers used in PCIe-FRM26_B will be described. The main connectors are SDR 26pin connectors J5, J6, and J8 connectors for Camera Link connection.

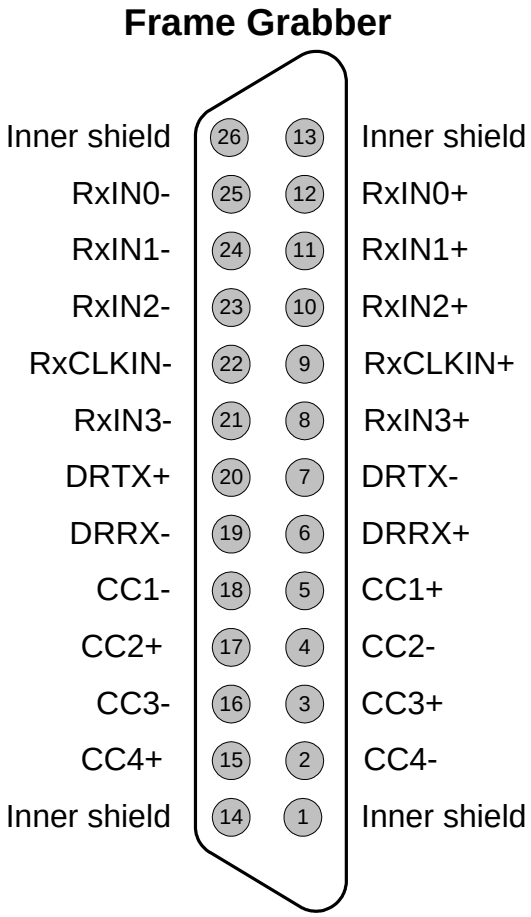
[Figure 3-2] shows the bracket that interfaces with the board and the connection connector.



[Figure 3-2. PCIe-FRM26_B Front View]

3-3-1 J5/J6/J8(SDR26) Connector

The figure below shows the pin map of the J5/J6/J8 connector of the board used when using the Base Configuration Camera Link. All pin specifications are input/output based on the Camera Link standard, so please refer to the Camera Link standard document for details.



[Figure 3-3. J5/J6/JJ8 Connector Pin-out]

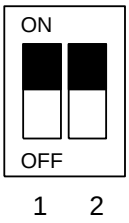
[Table 1. J5/J6/J8 Connector]

Pin No	Name	Description	Remark
1	Inner Shield	Cable shield	
2	CC4-	Camera Control output 4-	
3	CC3+	Camera Control output 3+	
4	CC2--	Camera Control output 2-	
5	CC1+	Camera Control output 1+	
6	DRRX+	Serial to Frame grabber +	
7	DRTX-	Serial to Camera-	
8	RxIN3+	Camera link LVDS receive data3 +	
9	RxCLKIN+	Camera link LVDS receive clock +	
10	RxIN2+	Camera link LVDS receive data2 +	
11	RxIN1+	Camera link LVDS receive data1 +	
12	RxIN0+	Camera link LVDS receive data0 +	
13	Inner Shield		
14	Inner Shield		
15	CC4+	Camera Control output 4+	
16	CC3-	Camera Control output 3-	
17	CC2+	Camera Control output 2+	
18	CC1-	Camera Control output 1-	
19	DRRX-	Serial to Frame grabber-	
20	DRTX+	Serial to Camera+	
21	RxIN3-	Camera link LVDS receive data3-	
22	RxCLKIN-	Camera link LVDS receive clock-	
23	RxIN2-	Camera link LVDS receive data2-	
24	RxIN1-	Camera link LVDS receive data1-	
25	RxIN0-	Camera link LVDS receive data0-	
26	Inner Shield		

(Note) For more information, refer to Camera Link Standard Specification.

3-3-2 J2 Connector

PCIE-FRM26_B board is designed to use up to 4 PCIe-FRM26_B boards simultaneously in one system (PC). Each board classification can be set through the 4-pin DIP switch in the board.



[Figure 3-3. J2 Connector (Top View)]

[Table 2. J2 PIN-OUT]

1	2	Description
OFF	OFF	Board No. 0
ON	OFF	Board No. 1
OFF	ON	Board No. 2
ON	ON	Board No. 3

3-3-3 J4 Connector

J4 is a JTAG (Joint Test Action Group) connector and is used to update the FPGA program on the board. Do not use when operating the board normally.

3-3-4 J7 Connector

It is a 3.3V external DC power connector. This is the power used when installing the FPGA and is not normally used.

4. Installation

4-1 Product Contents

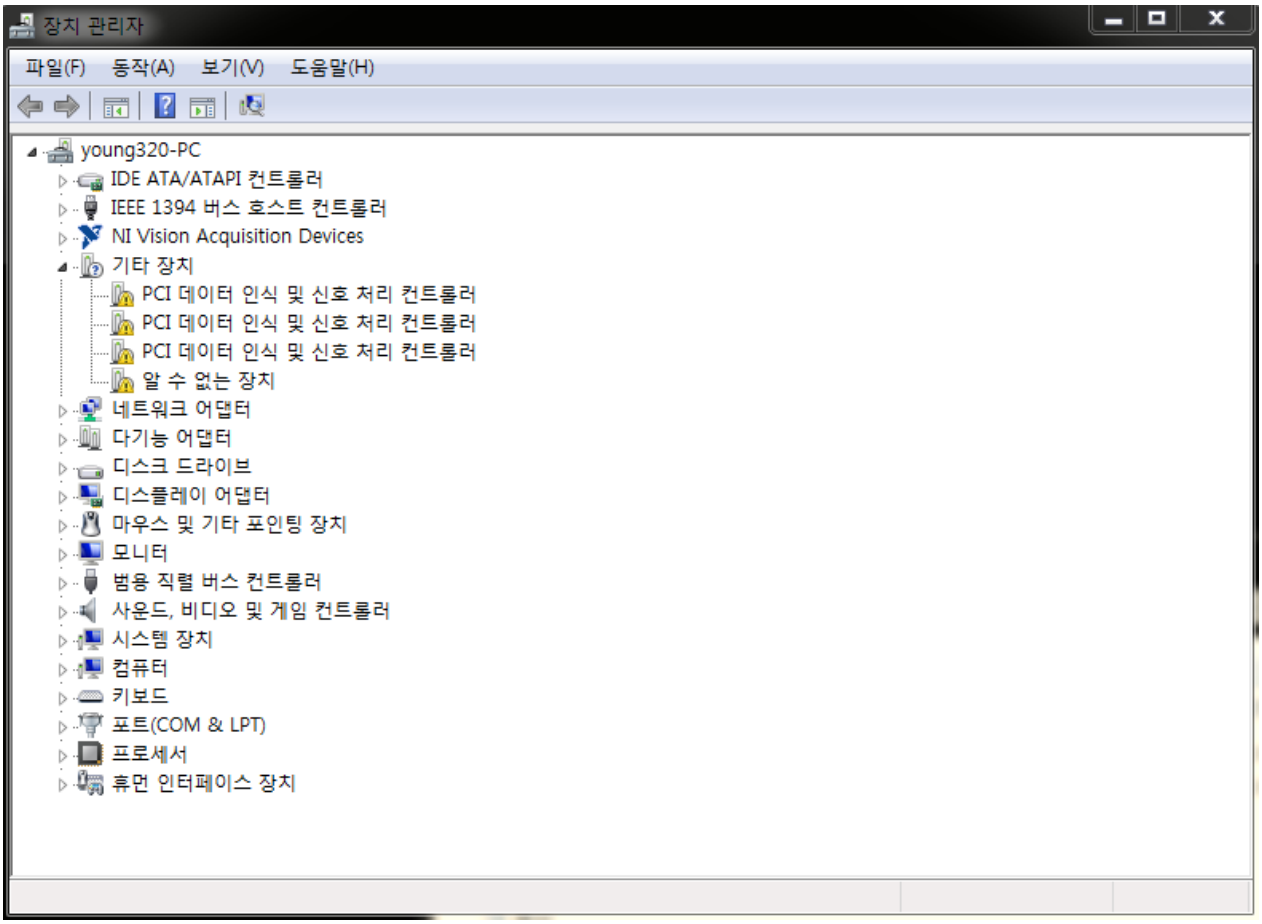
Before installing the board, check that the contents of the package are intact.

1. PCIe-FRM26_B Board
2. CD (Driver/Manual/API/Sample Source etc.)

4-2 Installation Process

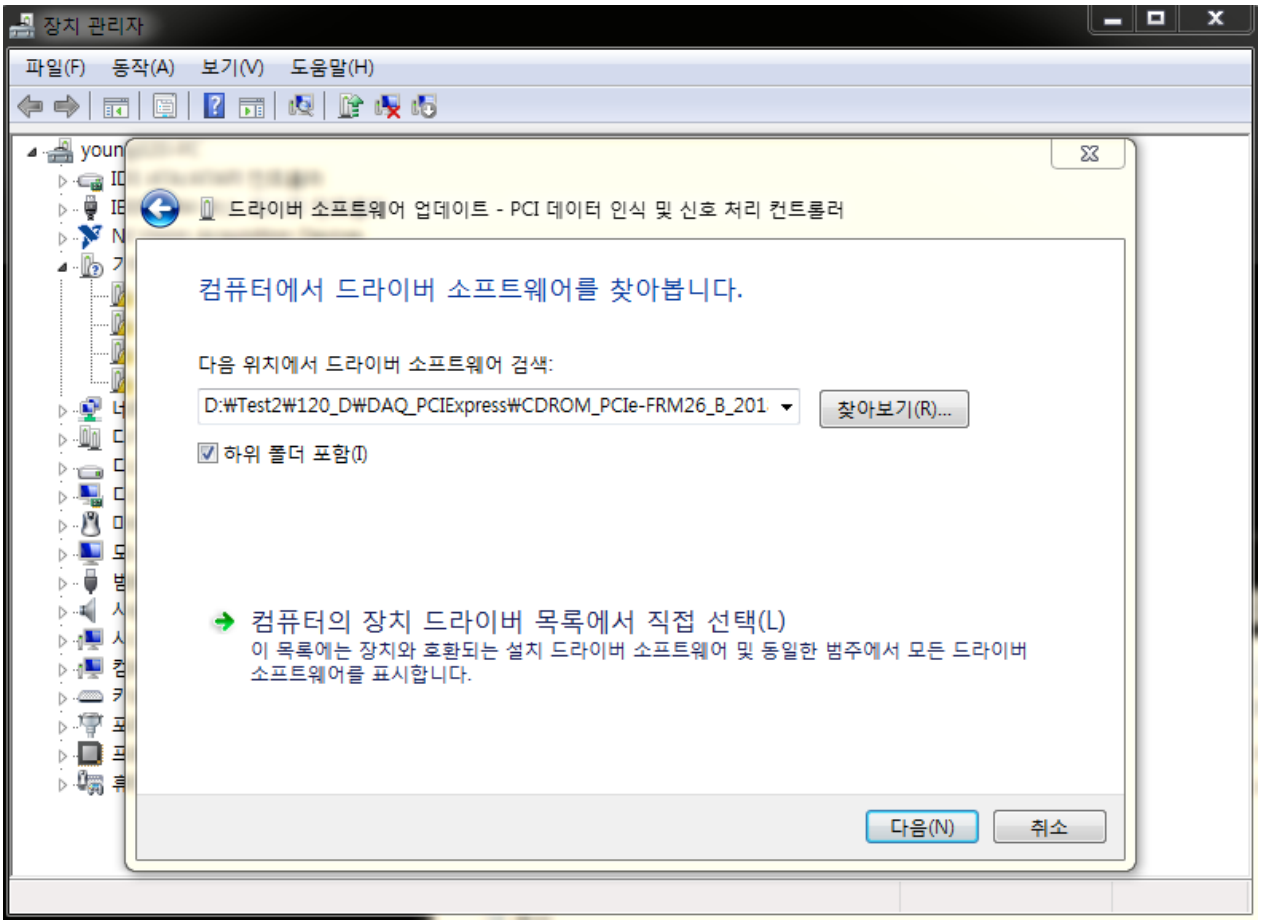
The board environment must be Windows 2000 SP4 or higher and Windows XP SP1 or higher. First, turn off the PC's power, plug the PCIe-FRM26_B board into the PCI Express Slot, and turn on the PC's power. When the "Start New Hardware Wizard" window opens as shown below, select it as shown below and click the Next button.

PCIe-FRM26_B recognizes each Base Configuration port as a driver. That is, as shown in the figure below, three devices are recognized and the installation process is performed three times.

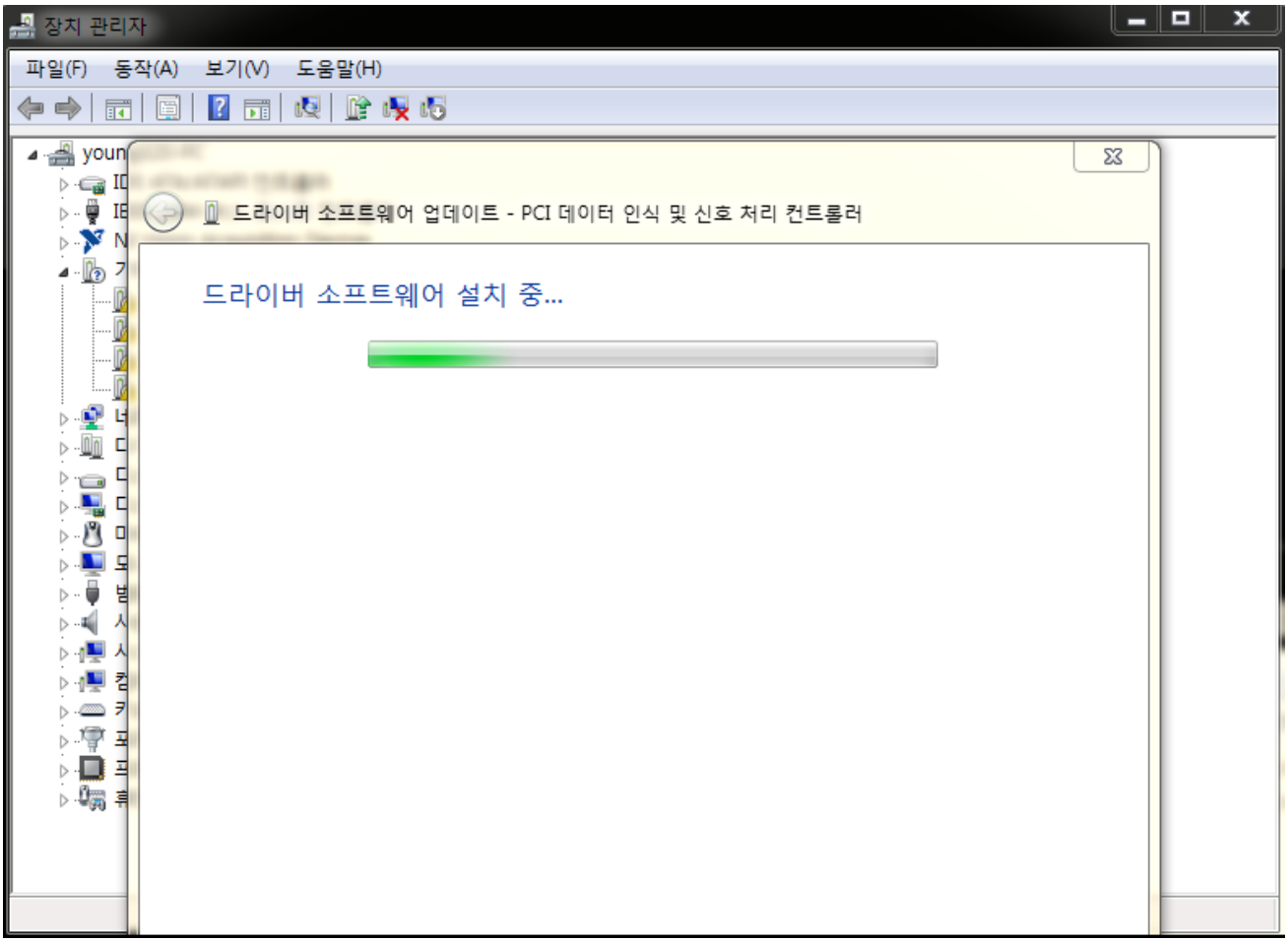


[Figure 4-1. "Device Manager" window]

1. Select Driver from the enclosed CD and click the Next button.

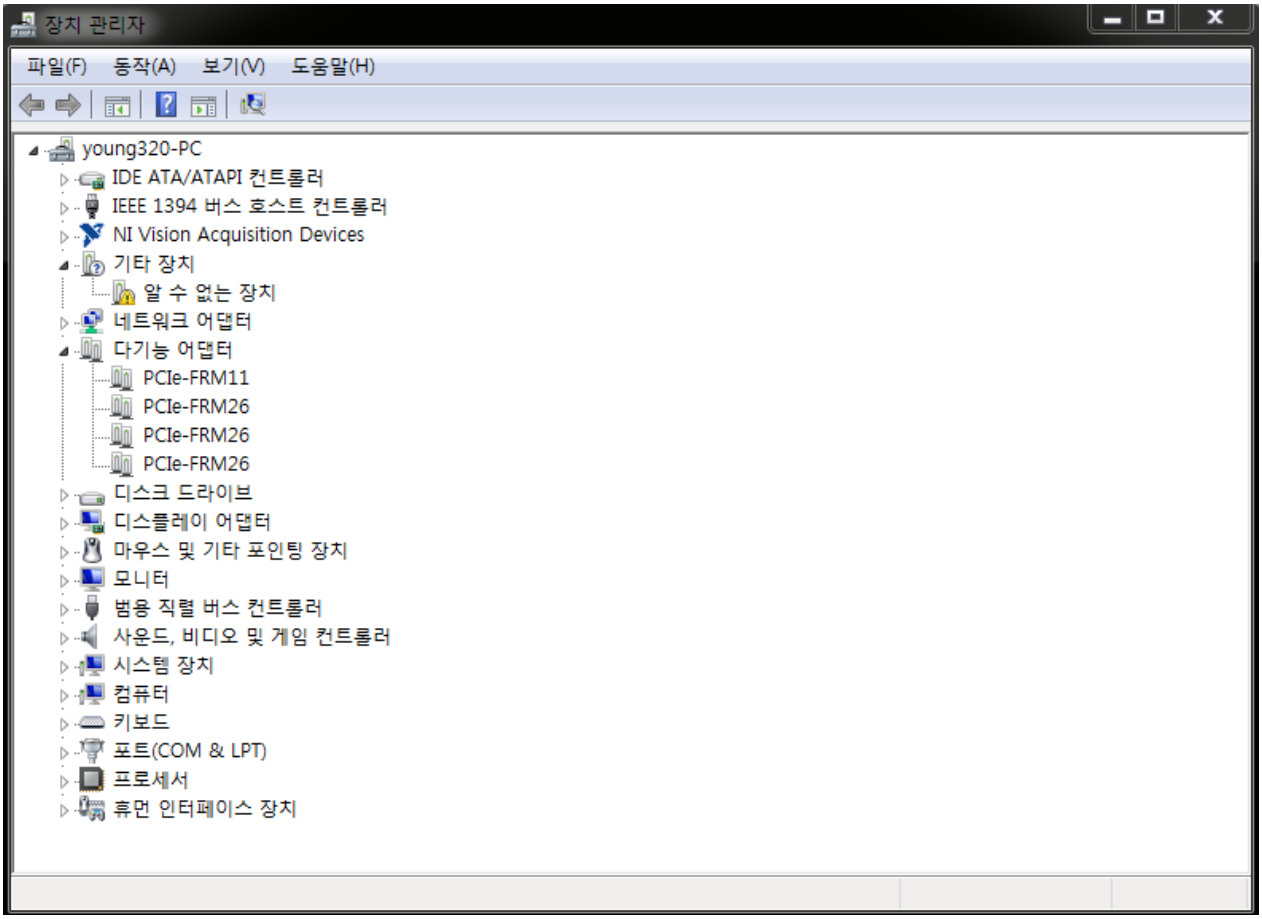


2. Click the Next button. It indicates that the installation process is proceeding as shown below.



3. When the installation is complete, check whether the driver is installed normally in the following way.

4. In My Computer -> Properties -> Hardware -> Device Manager, check if the **Multifunction Adaptor-> "PCIe-FRM26"** is installed.



The above figure shows the screen where the PCIe-FRM26_B board is normally installed in the PC.

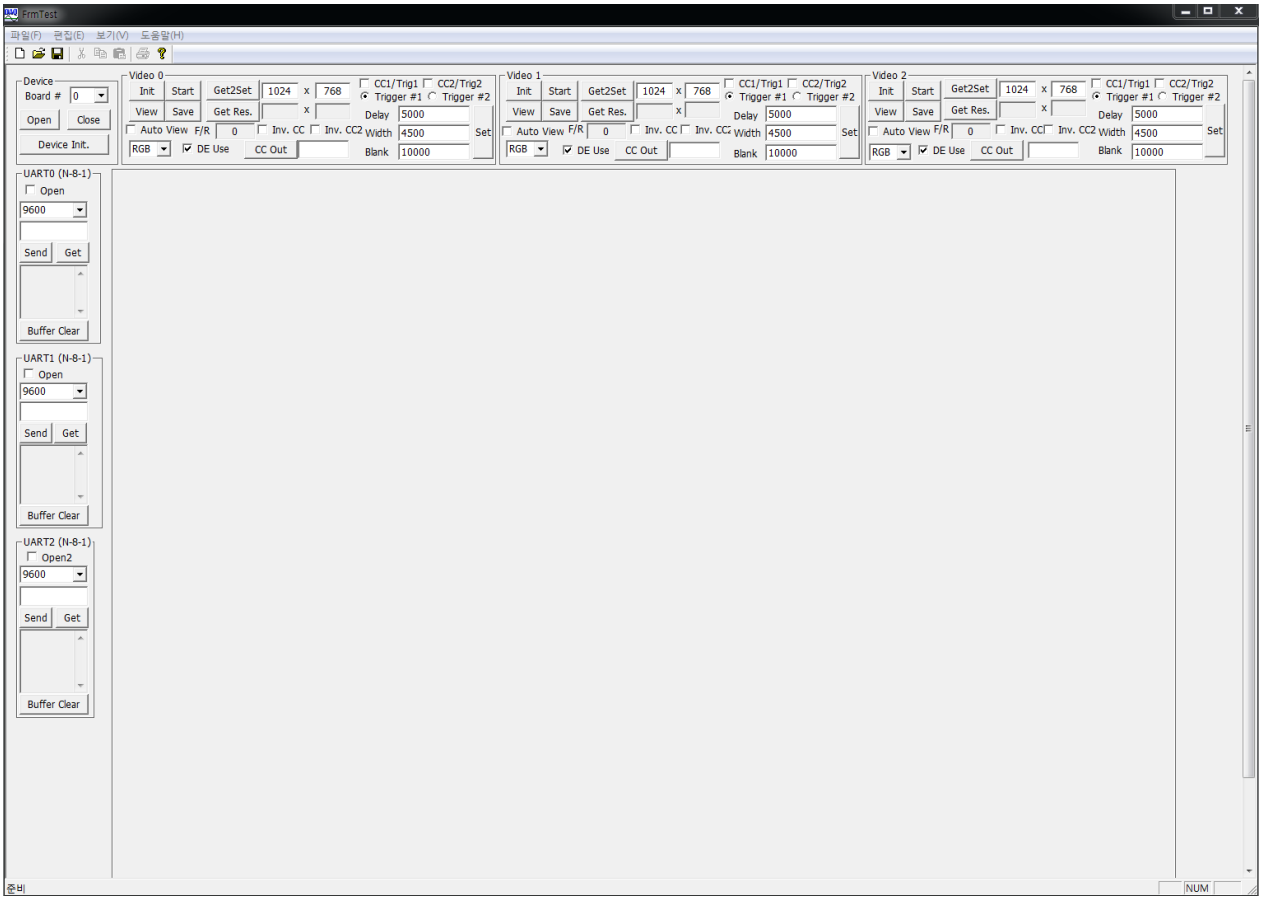
(Note) After initial installation, the PC must be rebooted for normal operation.

5. Sample Program

The TestApp folder on the CDROM supplied with the board provides a sample program "FrmTest" for easy use of the board. First, "FrmTest.exe", which is one of the executable files, displays frame data in hexadecimal value and stores it in memory or hard disk to utilize the frame data required by the developers. It is an executable file that shows the screen easily.

In order to test the sample program, the driver of the board must first be installed. The sample program is provided in source form so that the API provided for using the board can be briefly tested, so it can be modified and used by the user.

5-1 Image Frame Function



[Figure 5-1. Sample Program "FrmTest.exe"]

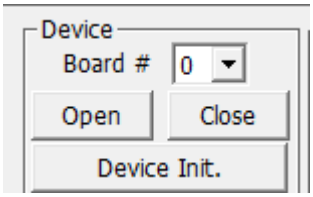
API (Application Programming Interface) is required to use the above sample program. API is provided in the form of "DLL", and import library and header file are required for compilation. All files specified above are included on the supplied CDROM. In order to run the sample program normally, the API DLL (PCI_FRM26B.dll) must be in the executable folder or in the Windows system folder or the folder specified by the Path environment variable.

In case of multi-board, two execution programs should be opened at the same time. Closing the program stops the remaining program operation. You need to run Device init and Start again.

Sample program execution sequence is as follows.

1. Get B'd # to determine the number of the board installed on the board
2. Select the board number for Board #.
3. Open ➔ Device Init ➔ Set the frame size to the specified resolution. (1024x768 setting)
4. Video0 ~ Video2: Start ➔ Start by selecting the number that matches the Base port you want to use.
5. Get Resolution ➔ Get2Set ➔ View (Still) or Auto View (Movie)
6. DE Use ➔ Depending on the sensor, the Data Valid signal may not be required.

The description of each menu bar is as follows. The menu bar not described here is an unused function.



(1) **"Board #" selection**

Four boards can be selected. Three devices are allocated per port on one board.
A total of 12 devices can be connected.

(2) **"Open" button**

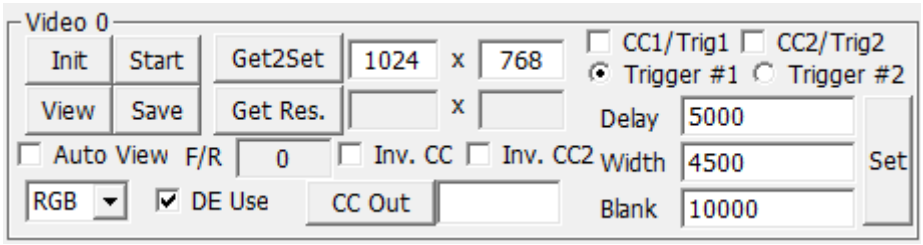
Start the device of the selected board.

(3) **"Close" button**

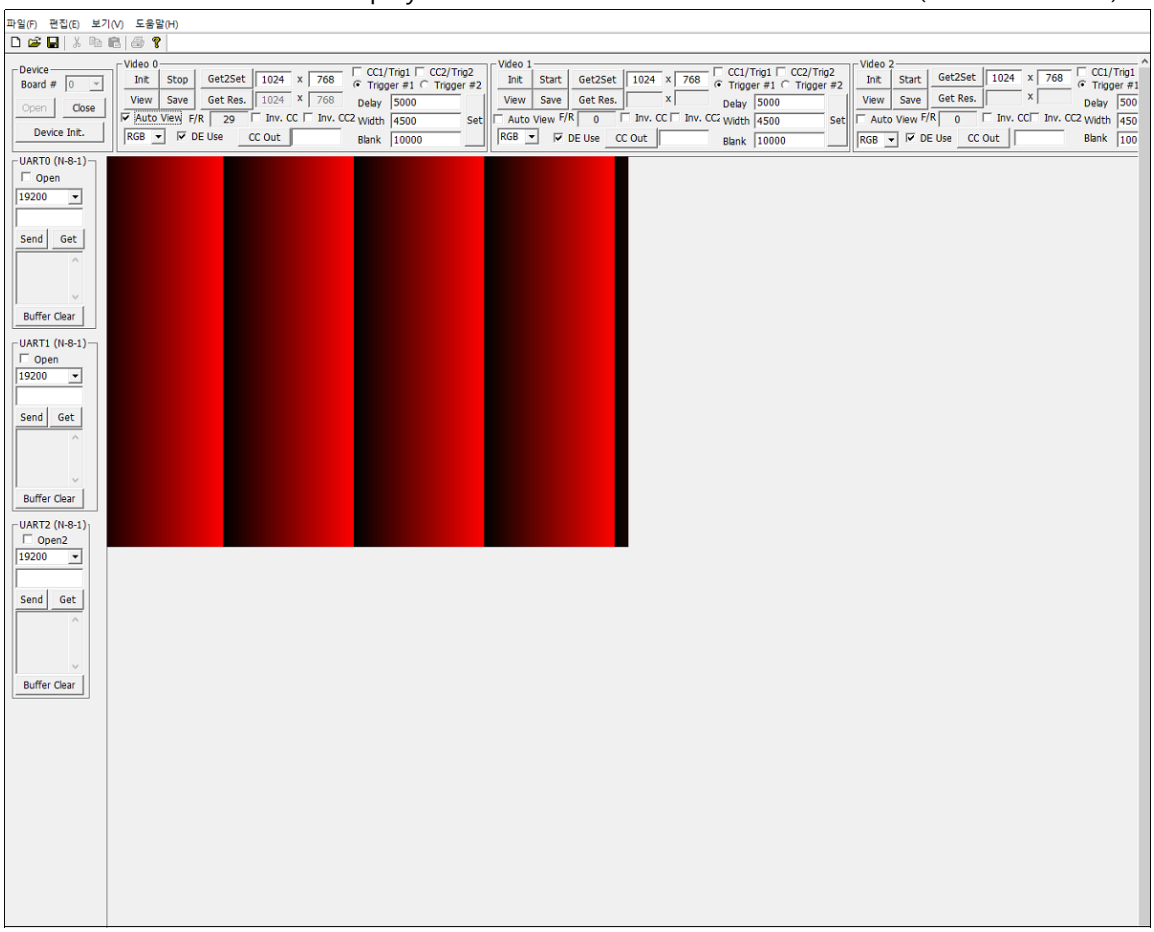
Close the device of the selected board.

(4) **"Device Init" button**

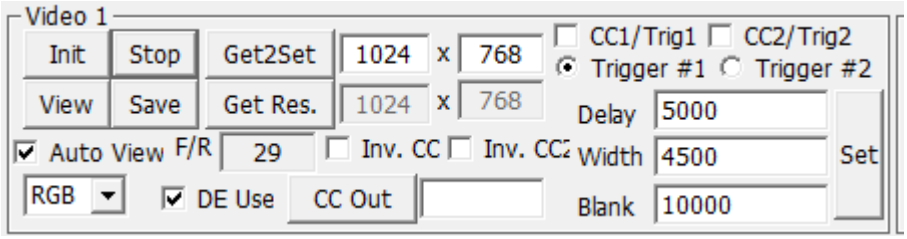
Initialize the image frame function. It is performed only once when the power is first applied.



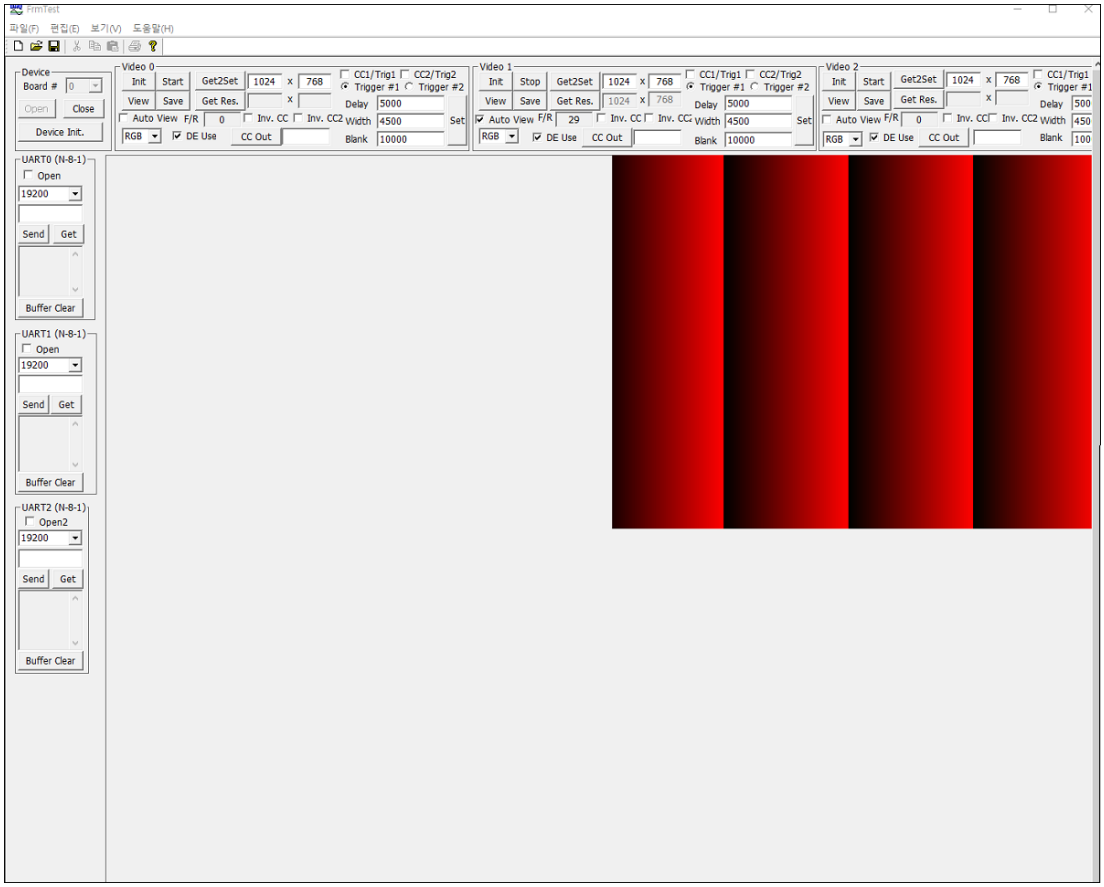
The Video 0 is the screen displayed when connected to the J8 connector. (See Section 3.3)



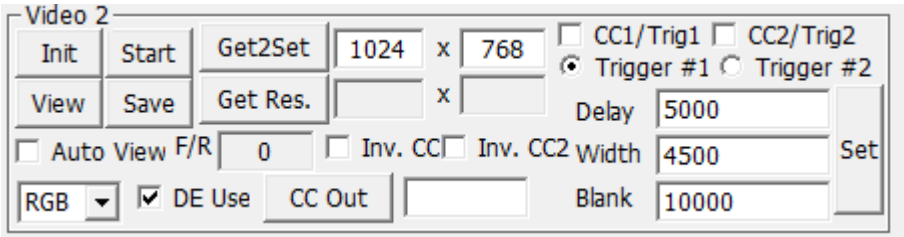
[Figure 5-2. Video 0 Display]



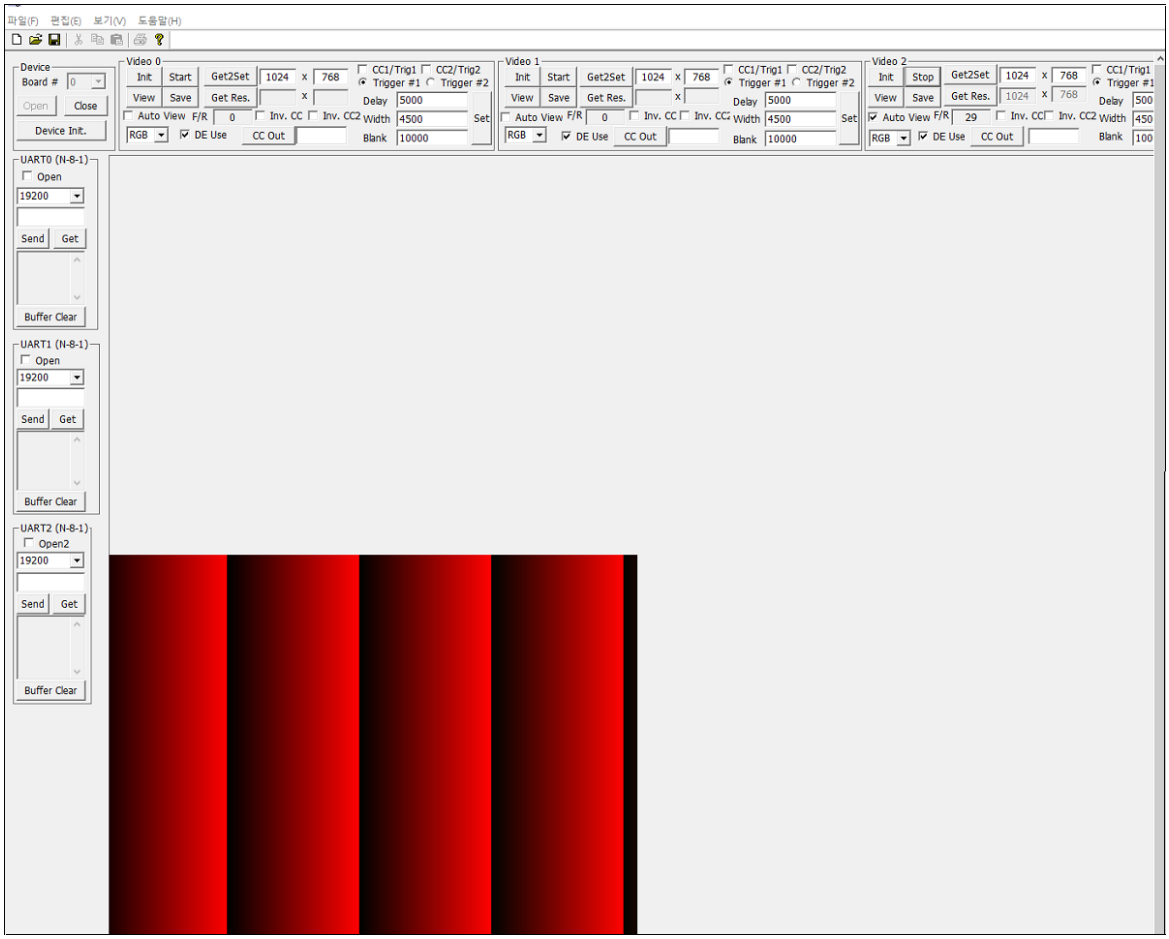
The Video 1 is the screen displayed when connected to the J5 connector. (See Section 3.3)



[Figure 5-3. Video 1 Display]



The Video 2 is the screen displayed when connected to the J6 connector. (See Section 3.3)



[Figure 5-4. Video 2 Display]

(5) **"Init " button**

It initializes a LVDS and UART.

(6) **"Video 0 F/R"**

It displays the frame rate per second.

(7) **"Start" button**

It starts transmission of images with "Start" and "stop" Toggle buttons.

(8) **"View" button**

The image frame stored on the board is read to the PC. If the image frame is not stored on

the board, you have to wait until the save is completed.

"Auto View": Show the video as checked.

(9) **"Save" button**

Clicking on the box will save the image data as a binary file in frame units.

(10) **"Get Res." button**

It displays the resolution of the input image.

(11) **"Get2Set." button**

It shows in the top column to set the input image resolution by "Get Res".

(12) **"RGB/YUV" selection**

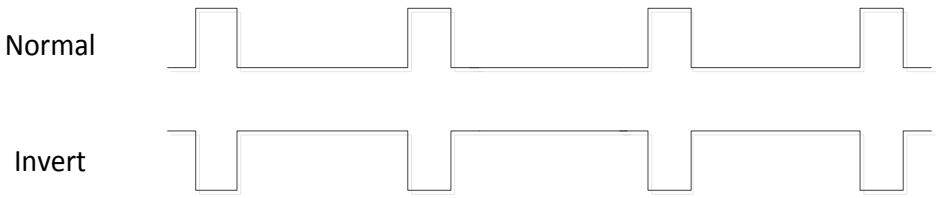
It selects RGB or YUV image signal.

(13) **"DE Use" selection**

It selects the Data Valid signal.

(14) **"Inv. CC" button**

Invert the selected CC1 or CC2 trigger pulse.



(15) **"CC Out"**

Called when writing a value to the general purpose I/O port.

The data value to be recorded is written in the editor box next to the button.

(Note) The range of data values to be recorded is 0x0 ~ 0F, in order from the lower bit to CC1, CC2, CC3, CC4.

(16) **"CC1/Trig1, CC2/Trig2" selection**

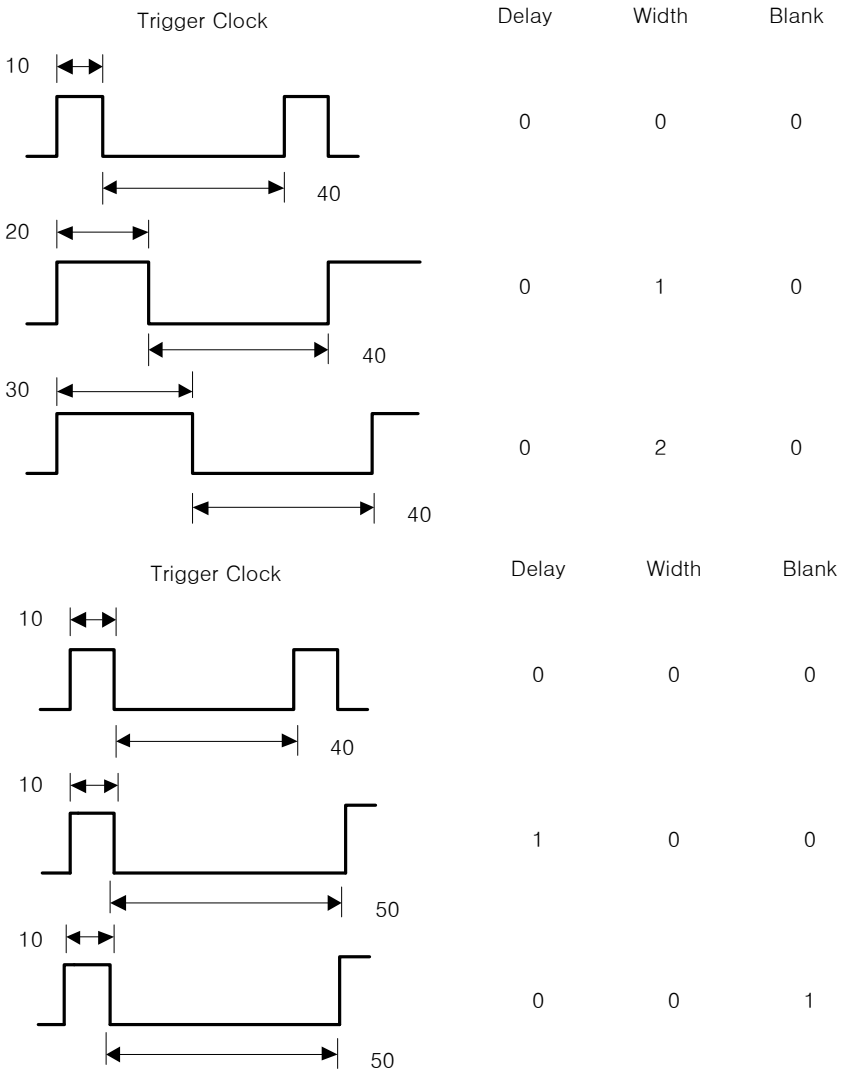
When checking, use CC1, CC2 as Trigger Mode. The setting method of Trigger Mode is as follows.

(17) **"Set" button**

Set the trigger Delay, Width, and Blank selected from Trigger #1 (CC1) and Trigger #2 (CC2). CC1 and CC2 can be used at the same time.

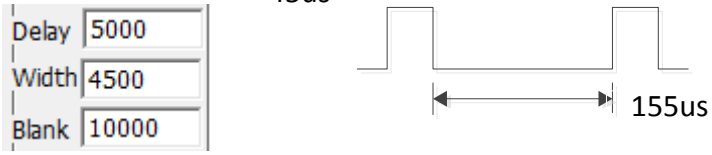
Delay & Width: 0 ~ 65535 Blank : 0 ~ 16777215 Total settable frequency is f = 1 / T, so 1 / ((65535 + 65535 + 16777215) * 10ns) = 0.17Hz.

Reference) If the default Delay/Width/Blank is set to 0/0/0, the total output is 50ns (10+40), so the maximum output is 20Mhz. The corresponding value increases by 10ns.



Increasing the Width increases the pulse width, and increasing Delay and Blank increases the interval.

For example, to use a trigger clock of 5000hz for CC1 or CC2, select CC from the "CC Cfg" button and set Delay/Width/Blank as follows.



Pulse Width = 4500 x 10ns = 45us
Pulse Delay + Blank = (5000 + 10000) x 10ns = 155us

5-2 UART Function

(1) **"Open" selection**

Normally UART Get is blocked and then clicked to open UART Get (For test)

(2) **"UART" selection**

It selects 9600, 19200, 38400, 57600, 115200 Baud Rate.

(3) **"UART Send" button**

It sends UART data in the above column..

(4) **"UART Get" button**

It gets data from the UART buffer.

(5) **"Buffer Clear" button**

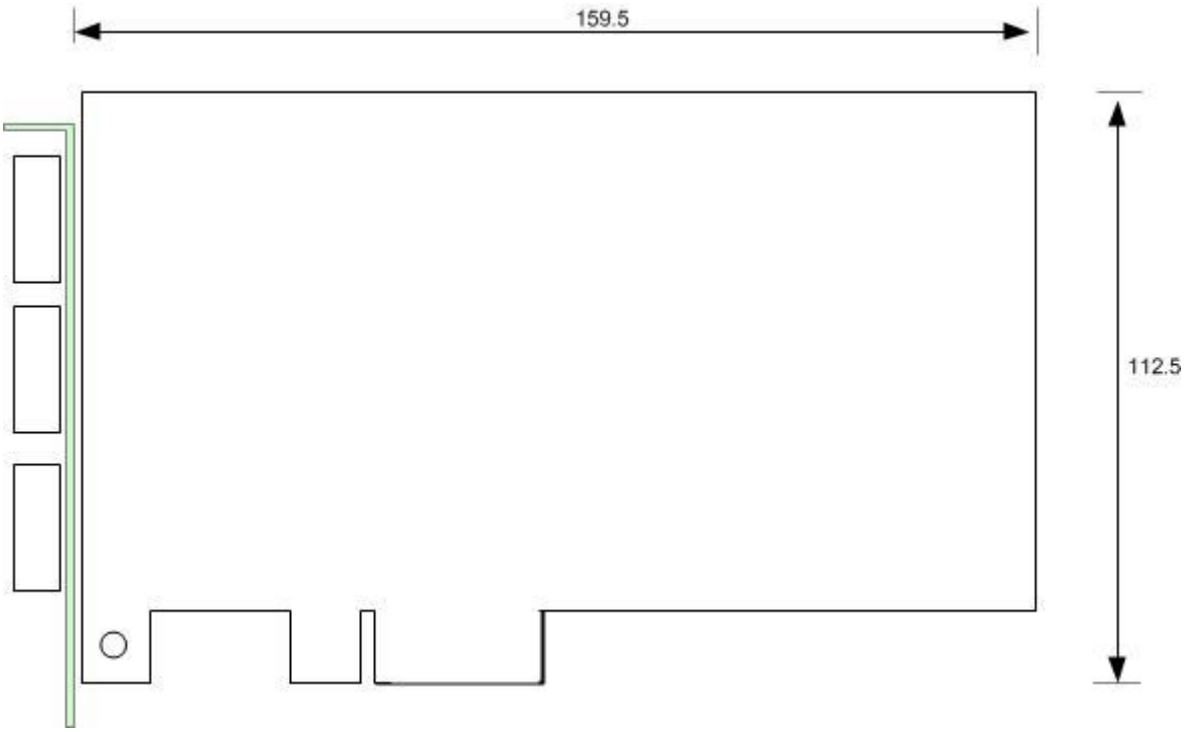
It clears the UART Receiver buffer.

Appendix

A-1 Board Size

The external sizes of the board are as follows.

For detailed dimensions, please contact the person in charge.



A-2 Repair Regulations

Thank you for purchasing a DAQSYSTEM product. Please refer to the following regarding Customer Service regulated by DAQSYSTEM.

(1) Read the user manual and follow the instructions before using the DAQSYSTEM product.

(2) When returning the product to be repaired, please write down the symptoms of the failure and send it to the head office.

(3) All DAQSYSTEM products have a 1-year warranty.
- -. Warranty period counts from the date the product is shipped from DAQSYSTEM.
- -. Peripherals and third-party products not manufactured by DAQSYSTEM are covered by the manufacturer's warranty..
- -. If you need repairs, please contact the Contact Point below..

(4) Even during the warranty period, repairs are charged in the following cases..
- ① Failure or damage caused by use without following the user's manual
- ② Failure or damage caused by customer's negligence during product transportation after purchase
- ③ Failure or damage caused by natural phenomena such as fire, earthquake, flood, lightning, pollution, or power supply exceeding the recommended range
- ④ Failure or damage caused by inappropriate storage environment (e.g. high temperature, high humidity, volatile chemicals, etc.)
- ⑤ Breakdown or damage due to unreasonable repair or modification
- ⑥ Products whose serial number has been changed or removed intentionally
- ⑦ If DAQSYSTEM determines that it is the customer's fault for other reasons

(5) Shipping costs for returning the repaired product to DAQSYSTEM are the responsibility of the customer.

(6) The manufacturer is not responsible for any problems caused by misuse, regardless of our warranty terms.

References

1. Specification of Camera Link Interface Standard for Digital Cameras and Frame Grabbers
-- Camera Link committee
2. PCI Local Bus Specification Revision2.1
-- PCI Special Interest Group
3. How to install PCI DAQ Board
-- DAQ system
4. AN201 How to build application using API
-- DAQ system
5. AN312 PCIe-FRM26_B API Programming
-- DAQ system
6. Camera Link
-- DAQ system

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Contact Point

Web sit : https://www.daqsystem.com

Email : postmaster@daqsystem.com

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Measurement & Automation