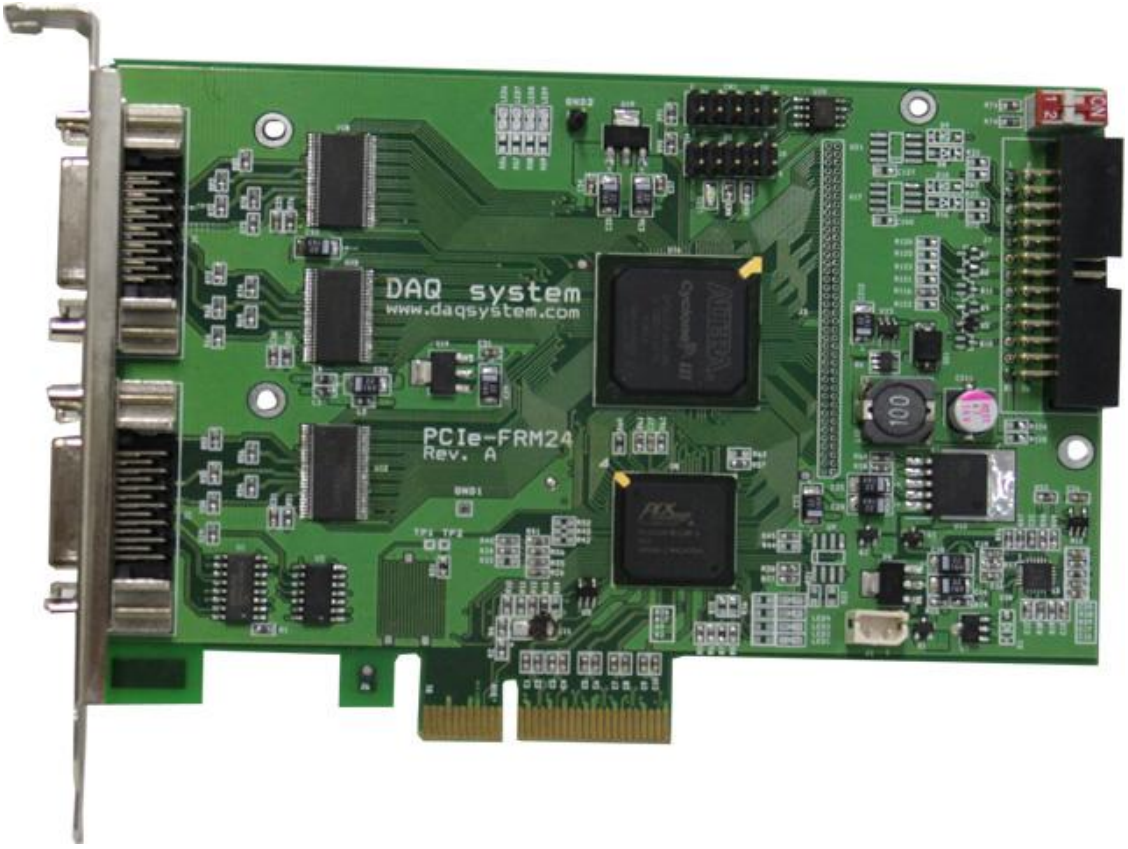
PCIe-FRM24

User's Manual

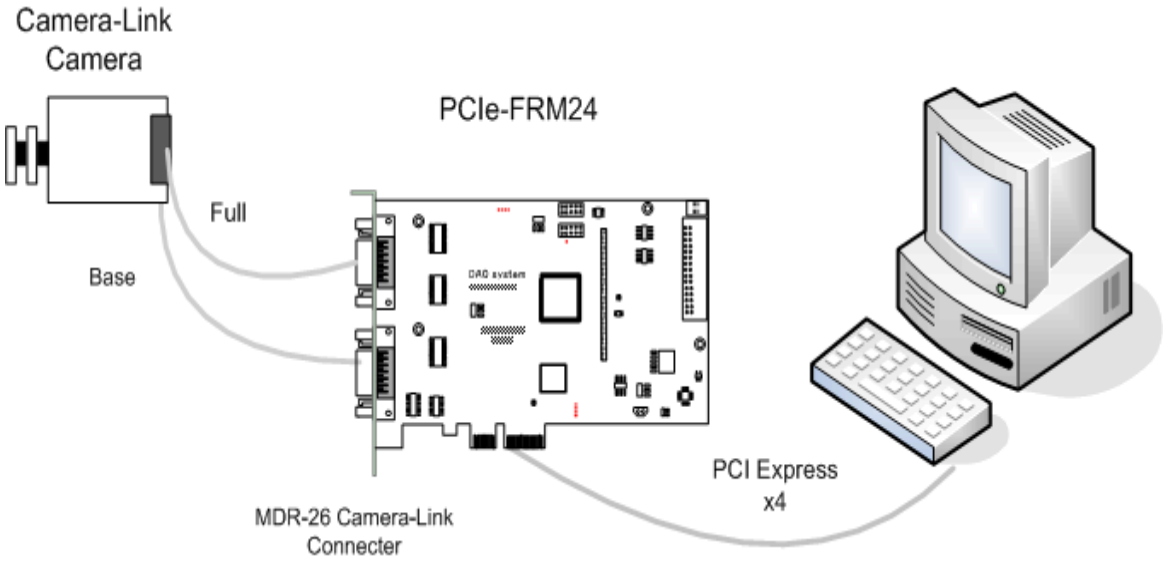


-- Contents --

1. Introduction

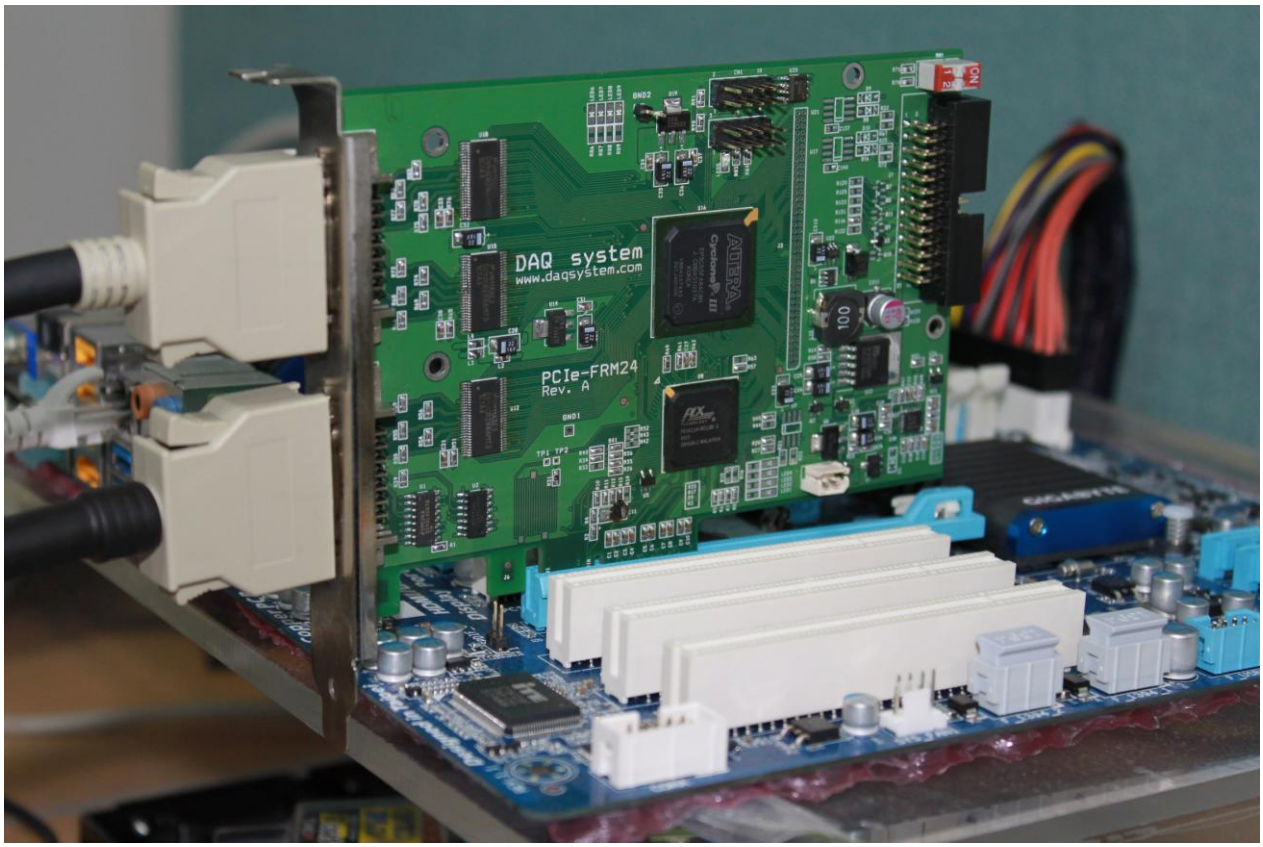
The PCIe-FRM24 is a board having the function of processing the frame data received from Camera-link camera and saving the image frame data in the system's main memory. It supports full Camera Link configuration, and Area Scan Camera, Line Scan Camera, Monochrome Camera Link Camera.

The operation of the board is controlled by program API, figure [1-1] shows connection of the system (usually PC).



[Figure 1-1. PCIe-FRM24 Board Usage]

As shown in Figure [1-1], the PCIe-FRM24 is inserted into any available PCI Express slot in your PC. It receives Image Frame from camera via Camera-Link Standard Interface. And, received data transmit to the API through PCI Express x4 interface.



[Figure 1-2. Picture of PCIe-FRM24 board real operation]

Figure [1-2] shows physical connection of the board to the Camera-Link Camera. At the left side, there are two Camera-Link connector and received image data (max. 680Mbyte).

[Features of the PCIe-FRM24]

- Support Base Configuration Camera Link
- Support Full/Medium Configuration Camera Link
- Support Line Scan & Area Scan Camera
- PCI Express 4x Interface
- Acquisition pixel clock rates up to 85MHz
- Video data rate of up to maximum 680Mbytes/sec
- UART(Data bit 8, 1 start, 1 stop, No parity, 9600/19200/38400/57600/115200bps) Rx/Tx
- External Device Interface : 4 TTL Digital Input/Output, and 2 TTL trigger Input Signals and 4-pair RS-422
- User Environment : Windows 2000 SP4, Windows XP SP1
- Convenient Windows Application Programming Interface(DLL)

[Application]

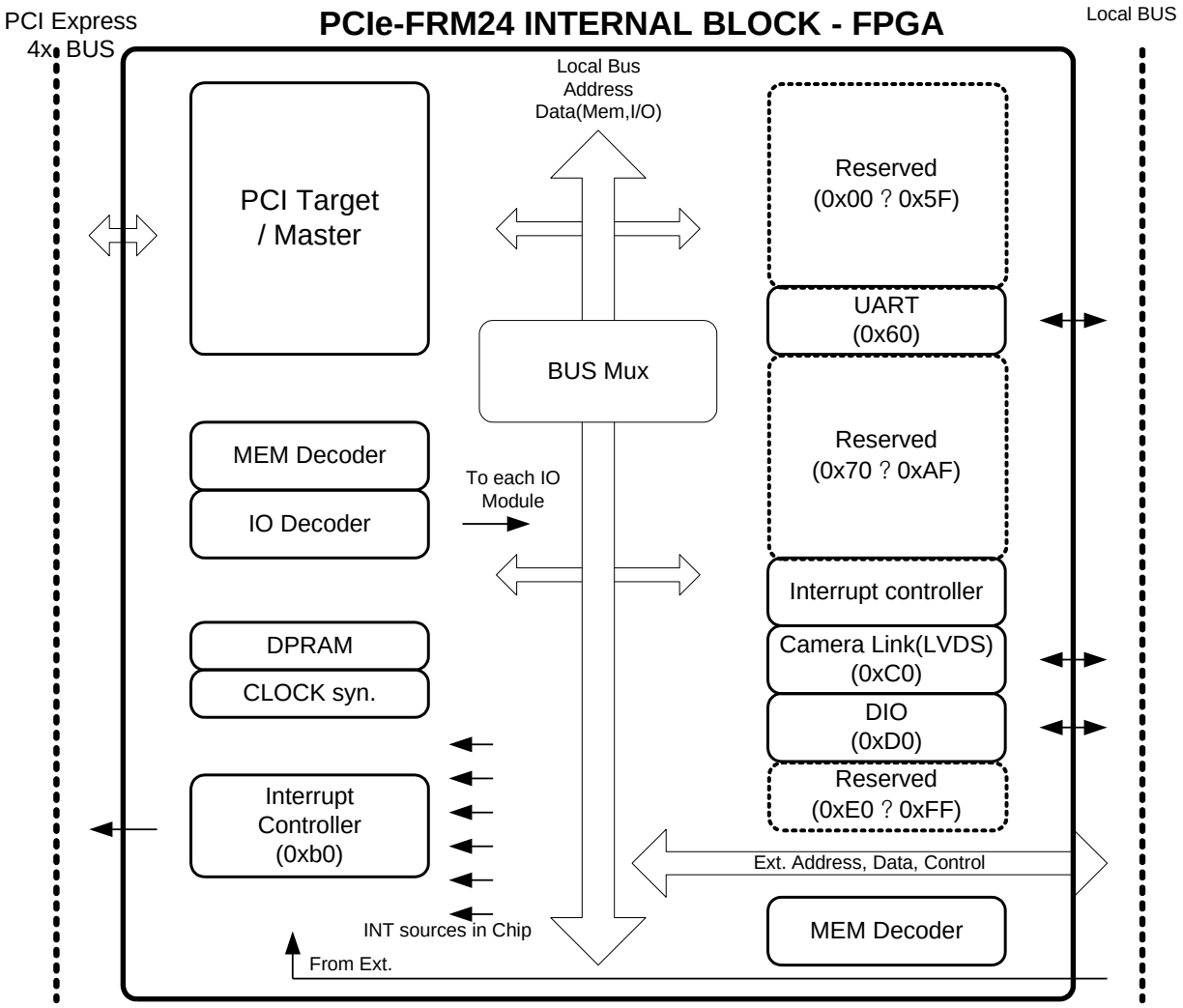
- Image Acquisition (Pattern, Particle etc.)
- Inspection Equipment (Sensor, Semiconductor, Device etc.)
- Security Solution
- Black and White, Color Image Display
- Medical Image Capture (X-ray, Supersonic etc.)

2. PCIe-FRM24 Functions

2.1 Block Diagram

As shown in the following figure, main control of the board is performed in FPGA Core Logic. Primary functions are receiving the image frame data, camera control signal and external Line Trigger I/O.

You can control these functions using API provided by DAQ system through PCI Express 4x interface.

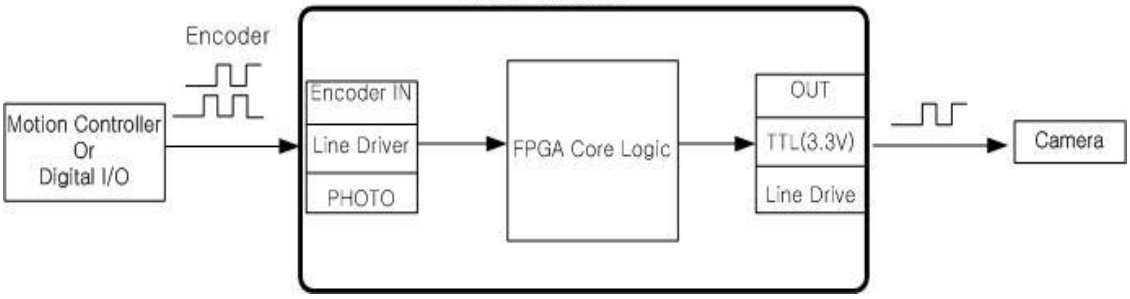


[Figure 2-1. Functional Block Diagram]

The core logic program of the FPGA is loaded by JTAG. It saves a program at the FPGA Program Logic and loads when power-up.

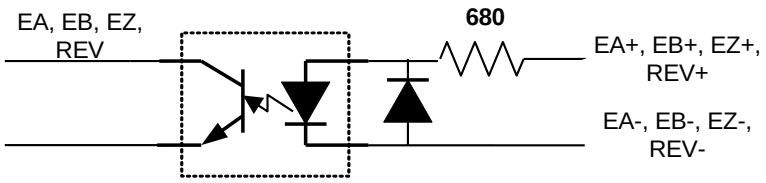
2.2 Encoder Trigger Controller

PCIe-FRM24 has 4 pair isolated photo-coupler input signals and 6 TTL level signals for external digital I/O (Motion Controller, Digital I/O board etc.). It can control a camera.



[Figure 2-2. Encoder Trigger Control]

[Figure 2-3] shows the Photo-coupler circuit. The output current has to be used under 10mA.



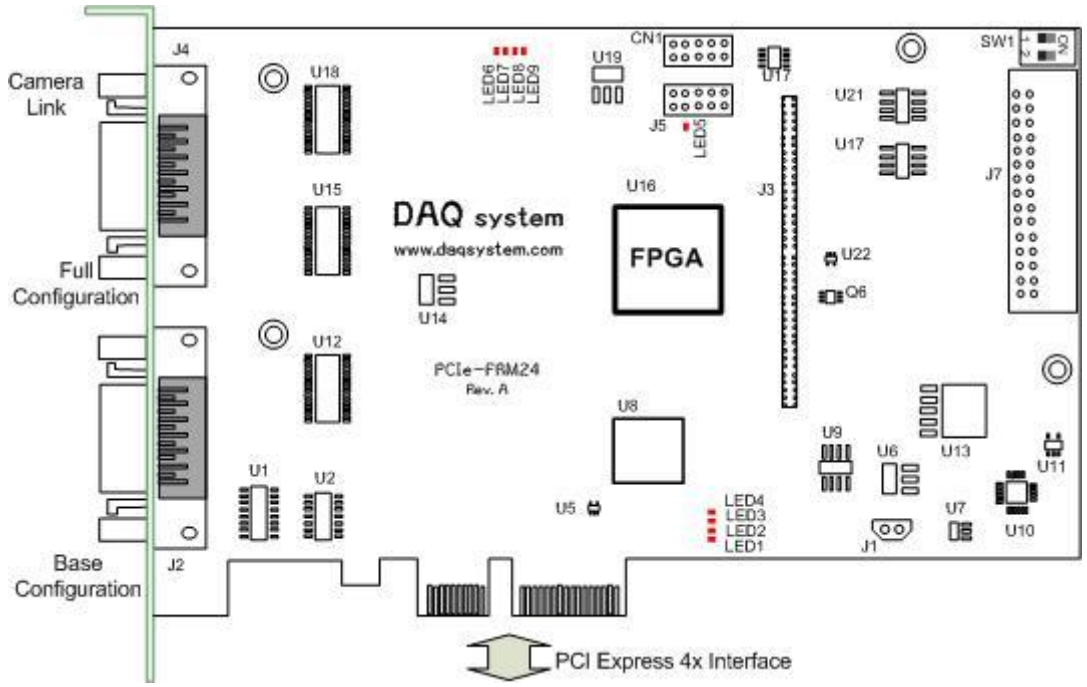
[Figure 2-3. Photo-coupler Circuit]

Caution) As Trigger Control can change according to kinds of Motion Controller or Camera, when you want use this function, contact to DAQ system

3. PCIe-FRM24 Board Description

In this chapter, the primary functions of the PCIe-FRM24 board are described briefly. For more information, refer to the device specification

3.1 PCIe-FRM24 Layout



[Figure 3-1. PCIe-FRM24 PCB Layout]

The board has five LEDs to indicate the operation status.

LED1 ~ LED4 turns on when PCI Express Lane (4 differential signal) is normal state.
LED5 turns on when power is applied to the board and the initialization ends up.
LED7 turns on when frame data is transferring. (When frame data is requested)
LED8 turns on when frame data is transferring. (When frame data is acquired)

3.2 Description of the functional blocks

(1) **MDR-26 Connecter : J2, J4**

Camera Link Base (J2), medium/Full (J4) Signal Connector

(2) **LVDS Link : U12, U15, U18**

Receive Image frame

(3) **FPGA : U16**

All of the board functions are controlled by the Logic program of the FPGA.

(4) **PCI Express Chipset: U8**

It ‘s a PCI Express Bridge.

(5) **Line Trigger : J7**

It is supposed to I/O circuit for external devices.

(6) **Regulator : U6, U7, U10, U11, U13, U20**

This block is for supplying the power to the board.

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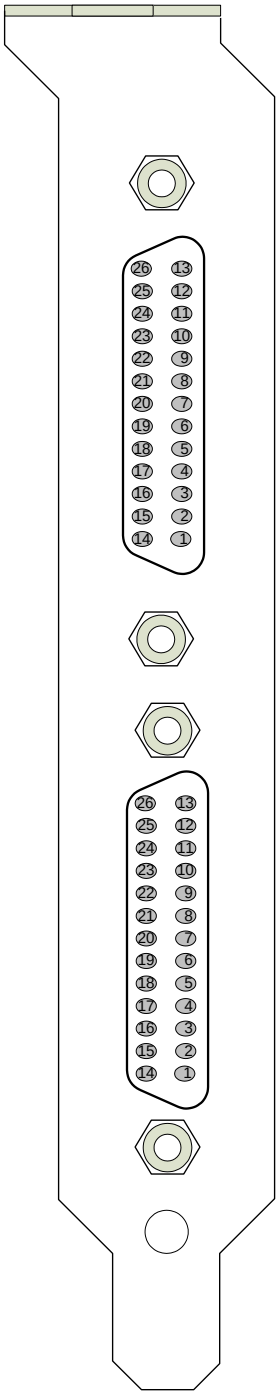
3.3 Connecter Pin-out

The PCIe-FRM24 board is equipped with MDR 26 Pin connector J2, J4 for Camera Link connection and 26pin Box Header connecter for external Trigger I/O.

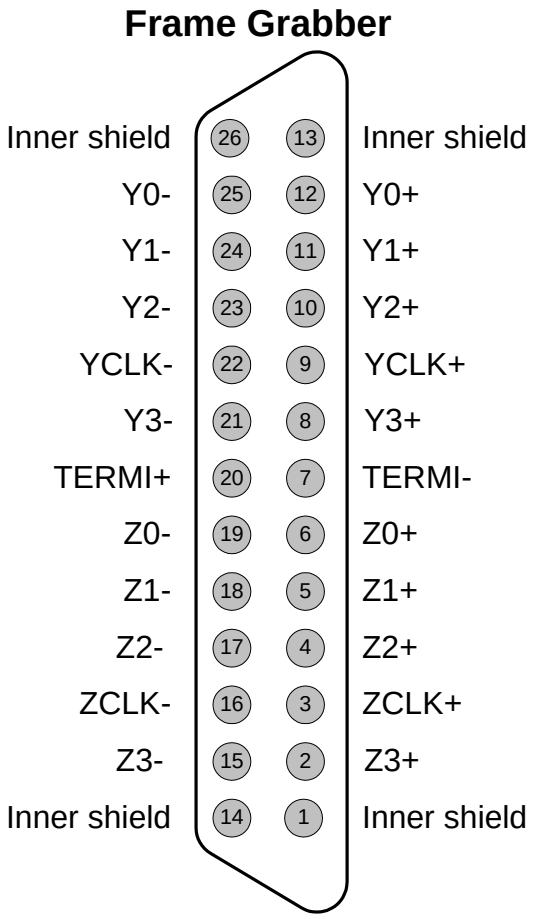
Figure [3-2] shows the bracket of the board and connector.



[Figure 3-2. PCIe-FRM24 Front View]

3.3.1 J4(MDR26) Connecter

Figure [3-3] shows the board's J4 connector pin-map when you use the Full Configuration Camera Link. All of the pin functions are based on the Camera link standard, so please refer to the Camera link standard document for more description and information.



[Figure 3-3. PCIe-FRM24 J4 Connector Pin-out]

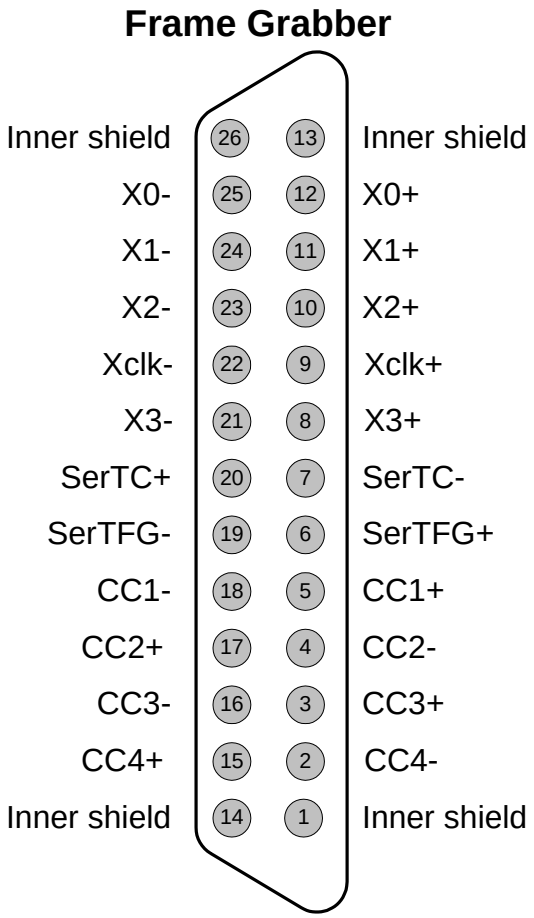
[Table 1. J4 Connecter Description]

Pin	Signal Name	Description	Remark
1	**Inner Shield**	Cable shield	
2	**Z3+-**	Camera link LVDS receive data11+	
3	**ZCLK+**	Camera link LVDS receive clock+	
4	**Z2+-**	Camera link LVDS receive data10+	
5	**Z1-**	Camera link LVDS receive data9+	
6	**Z0+**	Camera link LVDS receive data8+	
7	**TERMI-**	Serial to Camera-	
8	**Y3+**	Camera link LVDS receive data7 +	
9	**YCLK+**	Camera link LVDS receive clock +	
10	**Y2+**	Camera link LVDS receive data6 +	
11	**Y1+**	Camera link LVDS receive data5 +	
12	**Y0+**	Camera link LVDS receive data4 +	
13	**Inner Shield**		
14	**Inner Shield**		
15	**Z3-**	Camera link LVDS receive data11-	
16	**ZCLK-**	Camera link LVDS receive clock-	
17	**Z2-**	Camera link LVDS receive data10-	
18	**Z1-**	Camera link LVDS receive data9-	
19	**Z0-**	Camera link LVDS receive data8-	
20	**TERMI+**	Serial to Camera+	
21	**Y3-**	Camera link LVDS receive data7-	
22	**YCLK-**	Camera link LVDS receive clock-	
23	**Y2-**	Camera link LVDS receive data6-	
24	**Y1-**	Camera link LVDS receive data5-	
25	**Y0-**	Camera link LVDS receive data4-	
26	**Inner Shield**		

(Note) For more information, refer to Camera Link Standard Specification.

3.3.2 J2(MDR26) Connecter

Figure [3-4] shows the board's J2 connector pin-map when you use the Base Configuration Camera Link. All of the pin functions are based on the Camera link standard, so please refer to the Camera link standard document for more description and information.

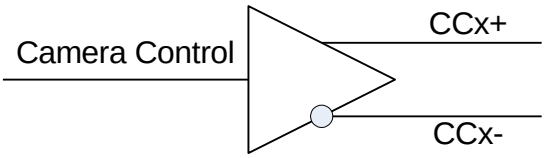


[Figure 3-4. PCIe-FRM24 J2 Connector Pin-out]

[Table 2. J2 Connecter Description]

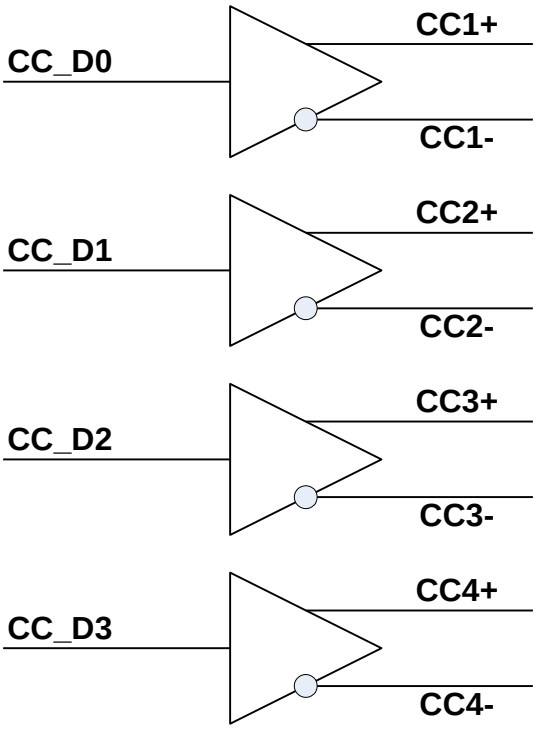
Pin	Signal Name	Description	Remark
1	**Inner Shield**	Cable shield	
2	**CC4+-**	Camera Control output 4+	Refer to Figure 3-5
3	**CC3-**	Camera Control output 3-	Refer to Figure 3-5
4	**CC2+-**	Camera Control output 2+	Refer to Figure 3-5
5	**CC1-**	Camera Control output 1-	Refer to Figure 3-5
6	**DRRX+**	Serial to Frame grabber +	
7	**DRTX-**	Serial to Camera-	
8	**RxIN3+**	Camera link LVDS receive data3 +	
9	**RxCLKIN+**	Camera link LVDS receive clock +	
10	**RxIN2+**	Camera link LVDS receive data2 +	
11	**RxIN1+**	Camera link LVDS receive data1 +	
12	**RxIN0+**	Camera link LVDS receive data0 +	
13	**Inner Shield**		
14	**Inner Shield**		
15	**CC4-**	Camera Control output 4-	Refer to Figure 3-5
16	**CC3+**	Camera Control output 3+	Refer to Figure 3-5
17	**CC2-**	Camera Control output 2-	Refer to Figure 3-5
18	**CC1+**	Camera Control output 1+	Refer to Figure 3-5
19	**DRRX-**	Serial to Frame grabber-	
20	**DRTX+**	Serial to Camera+	
21	**RxIN3-**	Camera link LVDS receive data3-	
22	**RxCLKIN-**	Camera link LVDS receive clock-	
23	**RxIN2-**	Camera link LVDS receive data2-	
24	**RxIN1-**	Camera link LVDS receive data1-	
25	**RxIN0-**	Camera link LVDS receive data0-	
26	**Inner Shield**		

(Note) For more information, refer to Camera Link Standard Specification.



Above picture is a Camera Control output circuit from PCIe-FRM24 board to Camera for the specific control of the Camera-link Cable.

The PCIe-FRM24 board has four differential digital outputs. Each output is mapped by Digital output. Below picture display that each bit position set.



[Figure 3-5. Camera Control LVDS Digital Output Circuit]

3.3.3 J1 Connector (2Pin Header, 2.54mm)

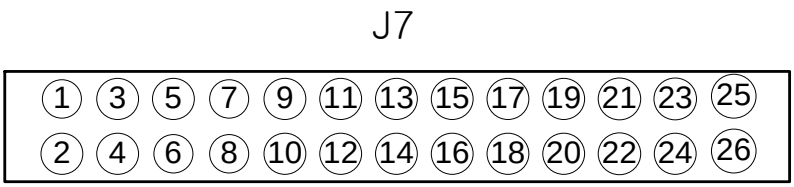
3.3V external DC power connector. It is a power source for FPGA installation and is not normally used.

3.3.4 J5 Connector

J5 is a Joint Test Action Group (JTAG) connector used to update the FPGA program on the board. It does not use when operating the board normally.

3.3.5 J7 Connector

J7 is an I / O connector that provides four pairs of isolated photo-coupler input signals, four TTL inputs, and two TTL output signal lines..



[Fig 3-5. J7 Connector (Top View)]

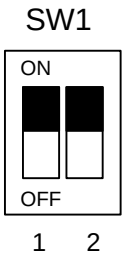
[Table 3. J7 PIN-OUT Description]

No.	Name	Description
1	**N.C.**	No Connection
2	**N.C.**	No Connection
3	**EA+**	Encoder A+ (Positive) Phase
4	**EA-**	Encoder A- (Negative) Phase
5	**EB+**	Encoder B+ (Positive) Phase
6	**EB-**	Encoder B-(Negative) Phase
7	**EZ+**	Encoder Z+ (Positive) Phase
8	**EZ-**	Encoder Z- (Negative) Phase
9	**REV+**	Direction (Positive) Signal
10	**REV-**	Direction (Negative) Signal
11	**PAGE_TRIGGER_IN**	TTL Input
12	**N.C.**	No Connection
13	**LINE_TRIGGER_START**	TTL Input
14	**N.C.**	No Connection
15	**DIGITAL_OUT**	TTL Output
16	**N.C.**	No Connection
17	**DIGITAL_IN**	TTL Input
18	**N.C.**	No Connection
19	**LINE_TRIGGER_IN**	TTL Input
20	**GND**	Ground
21	**LINE_TRIGGER_OUT**	TTL Output
22	**GND**	Ground
23	**N.C.**	No Connection
24	**GND**	Ground

25	**+3.3V**	Board Power (+3.3V)
26	**GND**	Ground

3.3.6 SW1

The PCIe-FRM24 board is designed of four maximum PCIe-FRM24 boards at the same time so as usable. Distribution of each board sets it up through 4 pin switch (SW1) in a board.



[Figure 3-6. SW2 Switch]

[Table 3. SW1 Description]

1	2	Description
OFF	OFF	Board No. 0
ON	OFF	Board No. 1
OFF	ON	Board No. 2
ON	ON	Board No. 3

4. Installation

4.1 Hardware Installation

In addition to the user's Manual, the package includes the following items. If any of these items is missing or damaged, contact DAQ system.

After unpacking, inspect the board carton to make sure there are no damages on the board.

4.1.1 Package Contents

① PCIe-FRM24 Board

② CD (Driver/Manual/API/Sample Source etc.)

- Document Folder : Manual and Catalog
- Driver Folder : pcie_frm24.sys, pcie-frm24.inf
- Sample Folder : Sample Application and DLL
- TestApp Folder : FrmTest.exe

4.1.2 Installation Process

① Turn off the PC power.

② Remove the computer cover using the instructions from the computer manual.

③ Insert the board empty PCI Express slot as soon as possible to close the CPU.

④ Remove the blank metal plate located at the back of the selected slot. Keep the removed screw to fasten the board after installation.

⑤ You should try number 3 in case of multi-board.

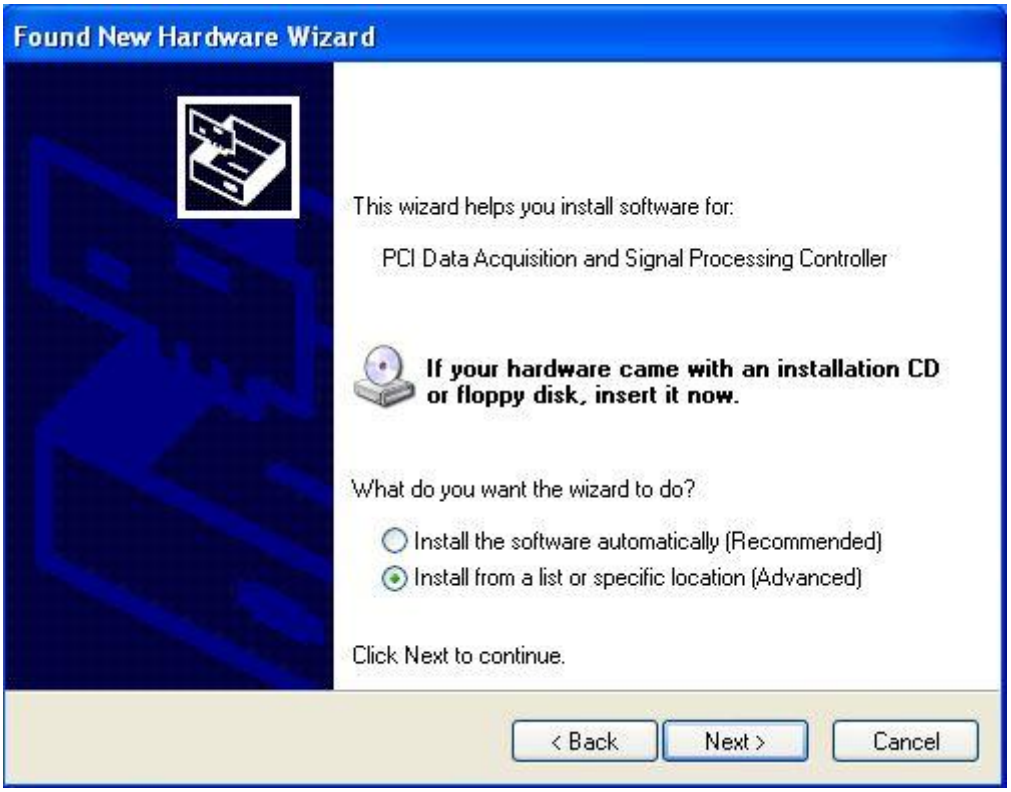
4.2 Software Driver Installation

To install your PCIe-FRM24 board in your PC, follow the steps described in the document "How to install PCI DAQ Board" provided by DAQ System. If the document is missing, you can get it from www.daqsystem.com. The PCIe-FRM24 board is completely Plug & Play. There are no switches or jumpers to set. Therefore you can install it easily.

- Your OS requirement : Windows 2000 SP4 or Windows XP SP1 above

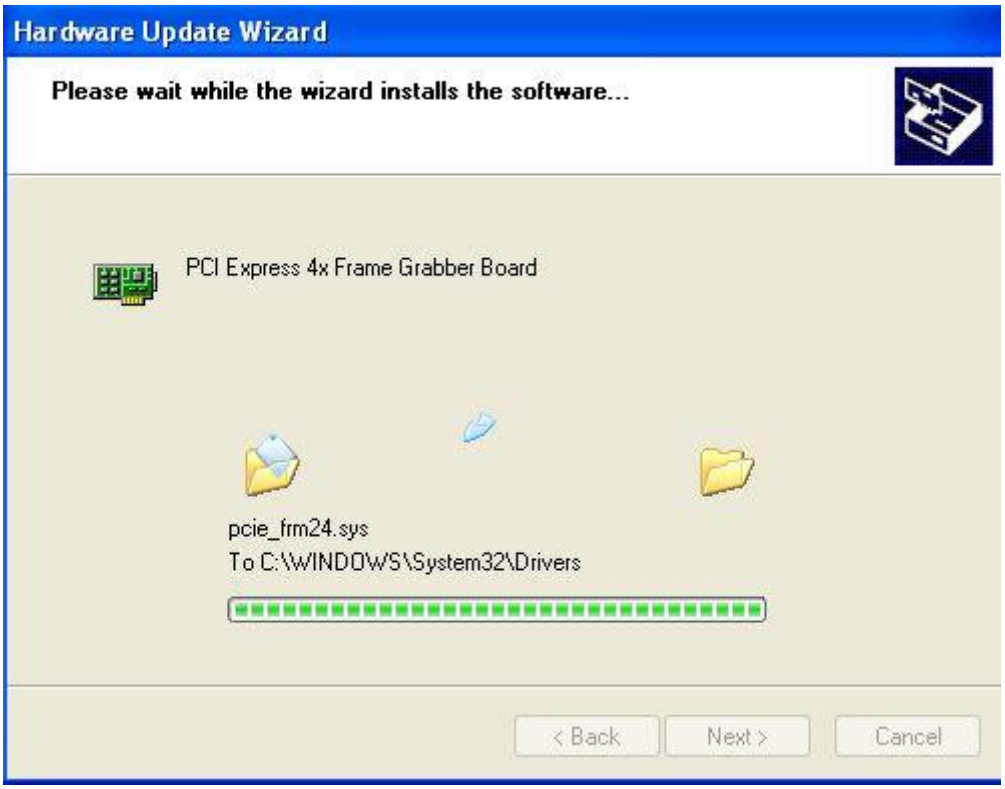
The PCIe-FRM24 connects to Express Card Port. After that you can show the below picture of "Welcome to found New Hardware Search Wizard" window.

If new hardware is found, Wizard will ask you to install the corresponding driver. For installation of the driver, select the item "Install from a list or specific location (Advanced)" and click "Next" as in the figure.



Select “Search for the best driver in these locations”. Check “Search removable media (floppy, CD-ROM)”. Check “include this location in the search”. Click “Browse” button. Select the folder where the drivers are located. Click “OK”. Click “Next”.

The necessary files are **“pcie_frm24.inf”** and **“pcie_frm24.sys”** in the driver polder.

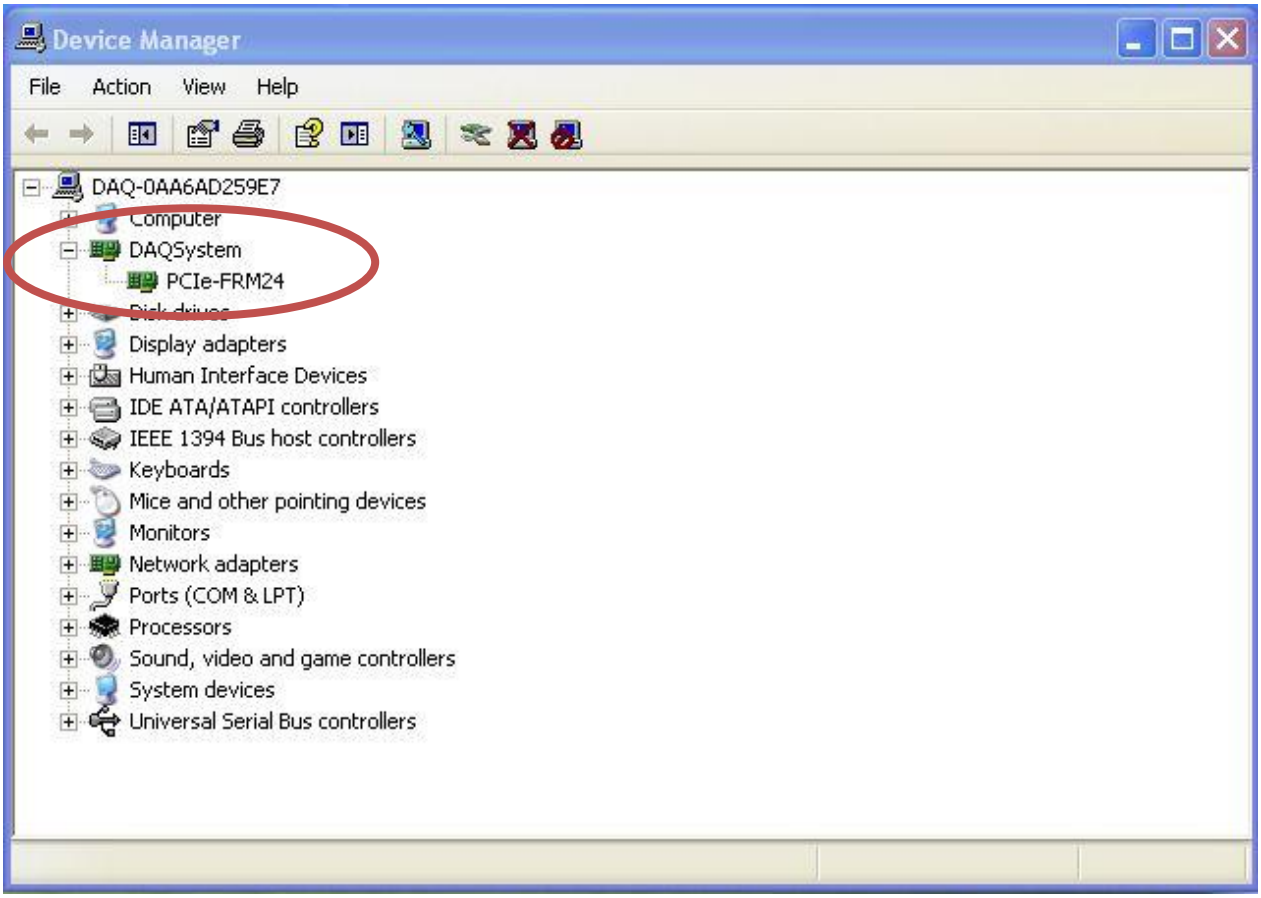

Hardware Update Wizard
Please wait while the wizard installs the software...
PCI Express 4x Frame Grabber Board
pcie_frm24.sys
To C:\WINDOWS\System32\Drivers
< Back
Next >
Cancel


Found New Hardware Wizard
Completing the Found New Hardware Wizard
The wizard has finished installing the software for:
PCI Express 4x Frame Grabber Board
Click Finish to close the wizard.
< Back
Finish
Cancel

If the installation is completely finished, you confirm it in the following ways.

Do the following steps to show up the “Device Manager” window.

[My Computer -> properties -> Hardware -> Device Manager -> **DAQSystem -> PCIe-FRM24**]



If you can see the “PCIe-FRM24” at Multifunction Adaptors, the driver installation is to have been over. (Check the red circle)

Important Notice : After installation, you should re-boot the system for the proper operation.

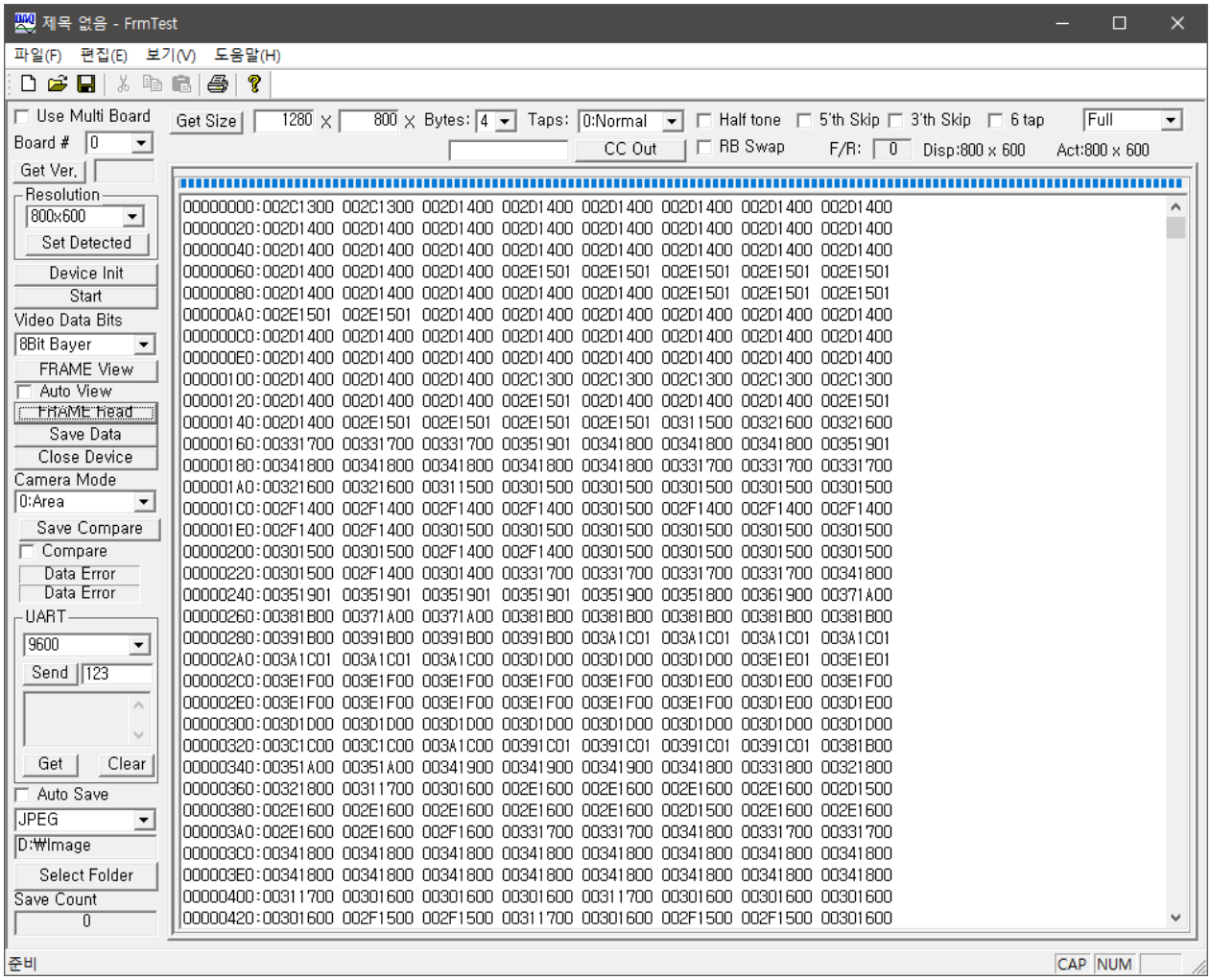
5. Sample Program

DAQ system provides a sample program to make the user be familiar with the board operation and to make the program development easier. You can find the sample program in the CDROM accompanying with the board.

One of the execution file is **"FrmTest.exe"**. It stores the frame data to memory or hard-disk and displays it to Hexa-decimal values which can utilize necessary frame data to developers. The other is **"FrameView.exe"**. It is easy to understand frame data to display the screen. Before using it, you have to install the PCIe-FRM24 board and its drivers in your computer.

Sample program is provided in source form in order to show the usage of API (Application Programming Interface) of the board and may be modified for customer's own usage.

5.1 FrmTest Program



[Figure 5-1. When Sample program "FrmTest.exe' is executed]

To run the sample application program, you need to use API, it is a form of client DLL. To compile the sample source to make its executable file, you have to use Import Library files and header files. You can find them in the CDROM. To run the .exe file, the API DLL file **(PCI_FRM24.DLL)** must be in the same directory with the .exe file or Windows system folder. Another method is to add the directory of API DLL file to PATH environmental variable. Figure [5-2] is a capture screen to execute "FrameView.exe". The image that is looked to a monitor as it accesses a Camera-Link connector to PCIe-FRM24 board.

Sample program execution sequence is as follows.

1. Select Bytes 1: 8bit, Bytes 2: 16bit, and Bytes 4: 32bit.
2. Get the resolution of the sensor with Get Size.
3. Resolution ➔ Select the resolution you want to display on the screen.
   Or select the resolution obtained from Get Size with Set Detected.
4. Device Init ➔ Set the frame size to the resolution of the sensor.
5. Start
6. Video Data Bits ➔ Select the type of input video
7. Frame View ➔ Actual frame driving function
8. Auto View ➔ Show the frame continuously.

Each menu bar explains as below explanation. It is not use a function without mention it.

(1) **"Board #" selection**

It can select a Board #0 ~ Board #3. (Selection J4)

(2) **"Get Ver."**

It indicates the FPGA version.

(3) **"Get Size."**

It gets the input resolution of the sensor.

(4) **"Bytes" selection**

Select the size of the data width. "0" means 8 bits, "1" means 16 bits, and "2" means 32 bits.

(5) **"Taps"**

Select camera mode. "0" indicates normal mode, and "1" indicates alternate mode.
(Not currently implemented.)

(6) **"Half tone" toggle**

Select Half tone mode.

"5th Skip": Skip 5th byte when selected. If Bayer is processed and shown on the screen, the 5th byte is not needed, so use it when removing it.

"3th Skip": Skip the third byte when selected.

(7) **"F/R"**

It displays the frame rate per second.

(8) **"Full/Top Left/Top Right/ Bot. Left/Bot. Right" selection**

Full shows the screen at 800x600 resolution, and the remaining selection shows enlarged image.

(9) **"Resolution"**

User can set up the resolution is 640x480, 800x600, 1024x768, 1280x720, 1280x1024, 1600x1200, 1920x1080, 1920x1200, 2048x1536, 2560x2048, 4080x2448.

"Set Detected" button: Returns to the resolution obtained from **"Get Size"..**

(10) **"Device Init" button**

Press this button to initialize the function of receiving image frame data. It is performed only once after power is applied to the board.

(11) **"Start" button**

Press this button to begin to save image data.

(12) **"Video Data Bits"**

It selects among of 8Bit, 16Bit YUV, 24Bit BGR, 8Bit Bayer, 10Bit Bayer.

(13) **"Frame View"**

When press this button, it displays a freeze-frame.

Auto View: When check this box, it displays a video

(14) **"Save Data"**

Press this button to begin to save image data.

(15) **"Close Device"**

Press this button to finish usage of the board and terminate the program.

(16) **"Camera Mode" selection**

0 : Area 1 : Line (Freerun) 2: Line (Ext) 3: Line (Int)

(17) **"Save Compare"**

"Compare" : Compares the original image file with the saved image file and displays the number of bytes incorrectly..

(18) **"UART" selection**

It selects 9600, 19200, 38400, 57600, 115200 Baud Rate.

(19) **"Send" button**

It sends UART data in the next column.

(20) **"Get" button**

It gets the data from UART buffer.

(21) **"Clear" button**

It clears the UART Receiver buffer.

(22) **"Auto Save"**

When checking, save the image file in BMP or JPEG format in the box below..

(Not currently implemented.)

(23) **"Select Folder"**

It selects the folder to save. By default, it is set to the D: \ Image folder.

"Save Count" : Displays the number of saved frame.

(24) **"CC" (Camera Control)**

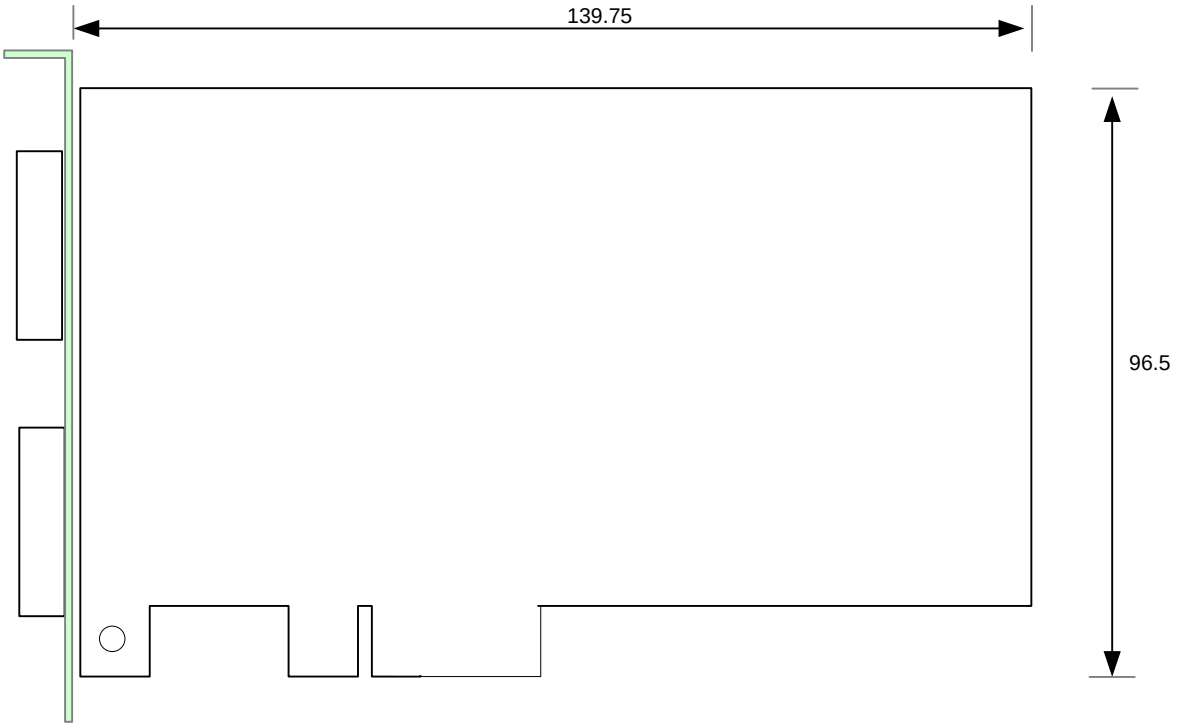
Camera Control can be set by the lower 4 bits of the left Edit Box.

Appendix

A.1 General Specification

Specification	
General	• PCI Express Specification Revision 1.0 • PCI Express 4x interface • Camera Link interface specification 1.0 and 1.1 • Support a Full Camera Link Interface • Two 26-pin (MDR-26) Connectors with full support of the "Full" Camera Link Specification • Video data rate of up to maximum 680Mbytes/sec • H/W and SDK is controlled by a programmable FPGA • Transmit Image Frame Data to PC
Software	
Supported OS	Windows XP/7/810
API	Interface with Application through client DLL
Sample Software	Test Sample software for evaluation

A.2 Physical Dimension (139.75 x 96.5 mm)



References

1. Specification of Camera Link Interface Standard for Digital Cameras and Frame Grabbers

-- Camera Link committee

2. PCI Local Bus Specification Revision2.1

-- PCI Special Interest Group

3. How to install PCI DAQ Board

-- DAQ system

4. AN201 How to build application using API

-- DAQ system

5. AN312 PCIe-FRM24 API Programming

-- DAQ system

6. Camera Link

-- DAQ system