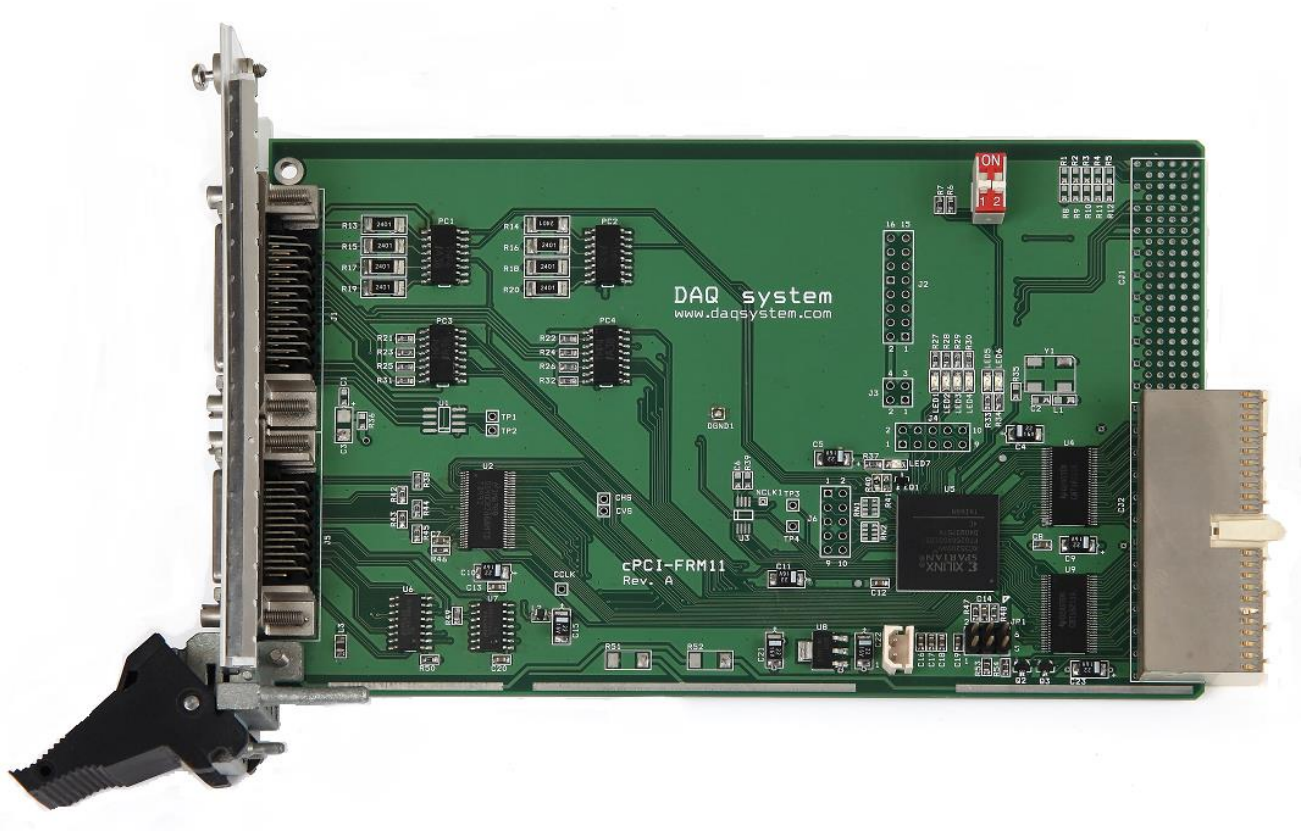
cPCI-FRM11

User Manual

Version 1.1



DAQ SYSTEM
Measurement & Automation

Contents

5. Sample Program

6. Test

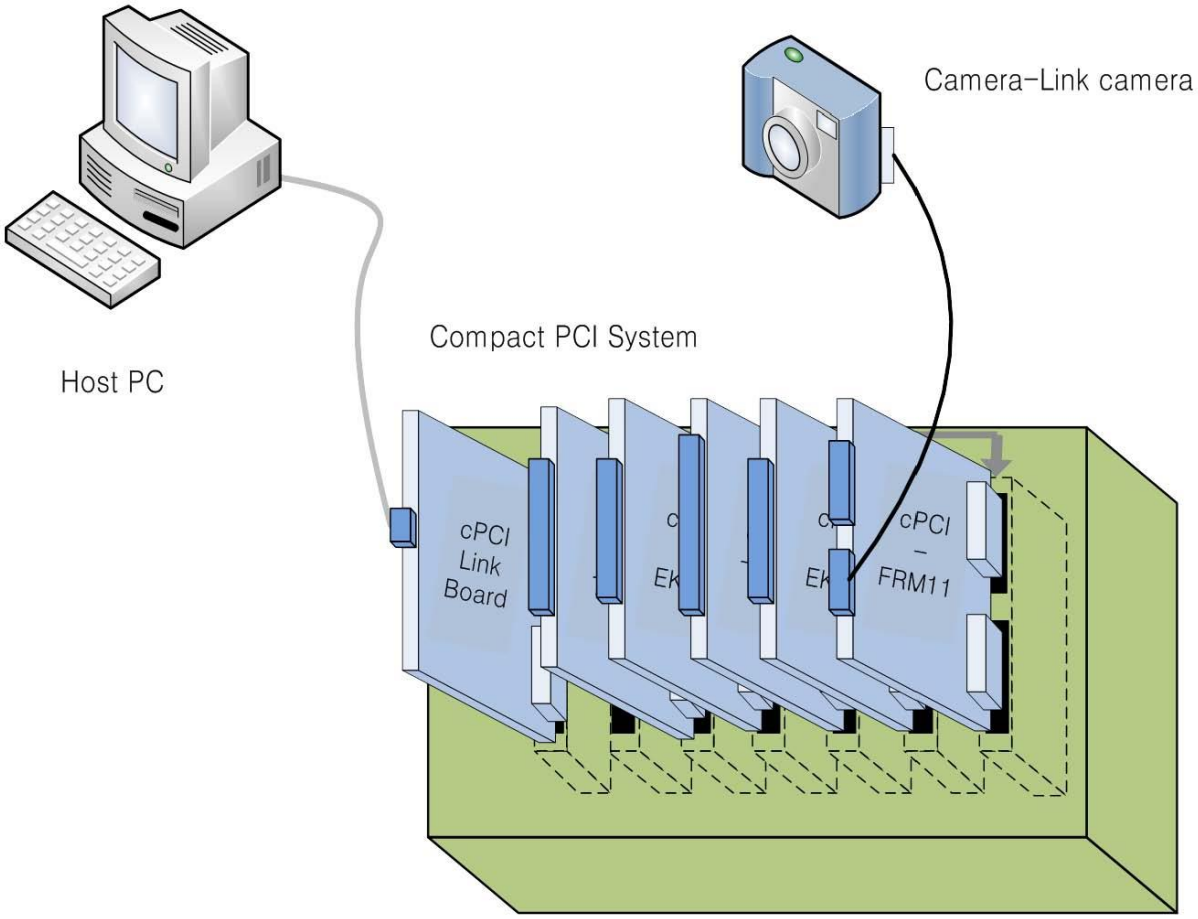
Appendix

References

1. Introduction

The cPCI-FRM11 is a board having the function of processing the frame data received from Camera-link camera and saves the data in the system's main memory. In addition, it supports Line Scan Camera and Area Scan Camera. It has the 8 digital inputs and 8 digital outputs for external controls and supports Trigger In/Out for RS-422 Interface.

The operation of the board is controlled by program API, figure [1-1] shows connection of the system.



[Figure 1-1. cPCI-FRM11 Board Usage

As shown in Figure [1-1], the cPCI-FRM11 is inserted into any available PCI slots in the Compact PCI system. It receives image frame from camera via Camera-Link Standard Interface. And, received data transmit to the API through PCI interface.

1-1 Product Features

Items	Description	Remark
Hardware		
PC Interface	Compact PCI	32bit/33MHz PCI Bus Interface
Operation Power	+5V Single Power operation Max within 300mA	
Video Interface	Base Camera Link	
Feature	Area Scan Camera Pixel Clock : 20 ~ 85MHz	
External I/O	8-Ch. Digital In 8-Ch. Digital Out	Digital Input : Voltage Range : 9 ~ 24V Current Range : 3.75mA (For 9V) ~ 10mA (For 24V) Digital Output : Voltage Range : ~ 7V Current Range : within 10mA
On-board Memory		
Communication	UART(Data bit 8, 1 start, 1 stop, No parity, 9600/19200/38400/57600 /115200bps)	
Simultaneous use of boards	Max. 4	
Software		
OS	Windows 2000/XP/7/8/10 (32/64bit)	
API	Windows Client DLL API	
Development		
Support	Sample Program	VC++
Environmental conditions		
Operating temperature range	0 ~ 60℃	
Storage temperature range	-20 ~ 80℃	
Humidity range	5 ~ 95%	Non-condensing
Board size	120.8mm X 68mm	PCB Board Size

1-2 Product Applications

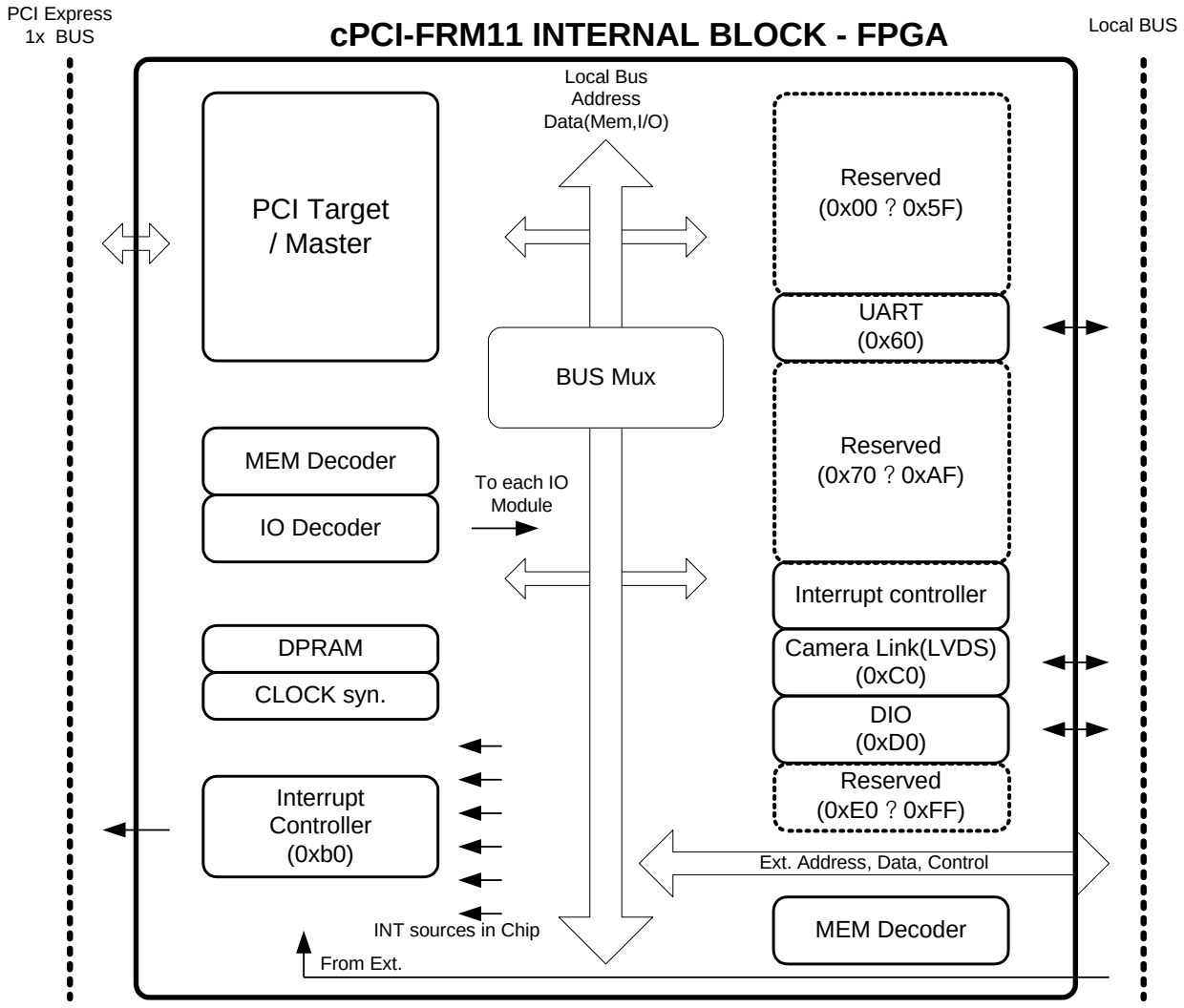
- Image recognition (Pattern, particle, etc.)
- Inspection equipment (Sensor, Semiconductor, Device etc.)
- Black and White, Color Image Display
- Medical Image Capture (X-ray, Supersonic etc.)

2. cPCI-FRM11 Board Function

2-2 Board Block Diagram

As shown in the figure below, in the case of cPCI-FRM11, FPGA Core Logic is in charge of overall control. Main functions include Frame Data reception, UART data transmission/reception for this purpose, and Camera Control signal output.

These functions are performed using API in PC through PCI interface.



[Figure 2-2. cPCI-FRM11 FPGA Block Diagram]

The FPGA core logic is programmed using JTAG, and the logic program is saved in FPGA Program Logic and loaded when power is applied.

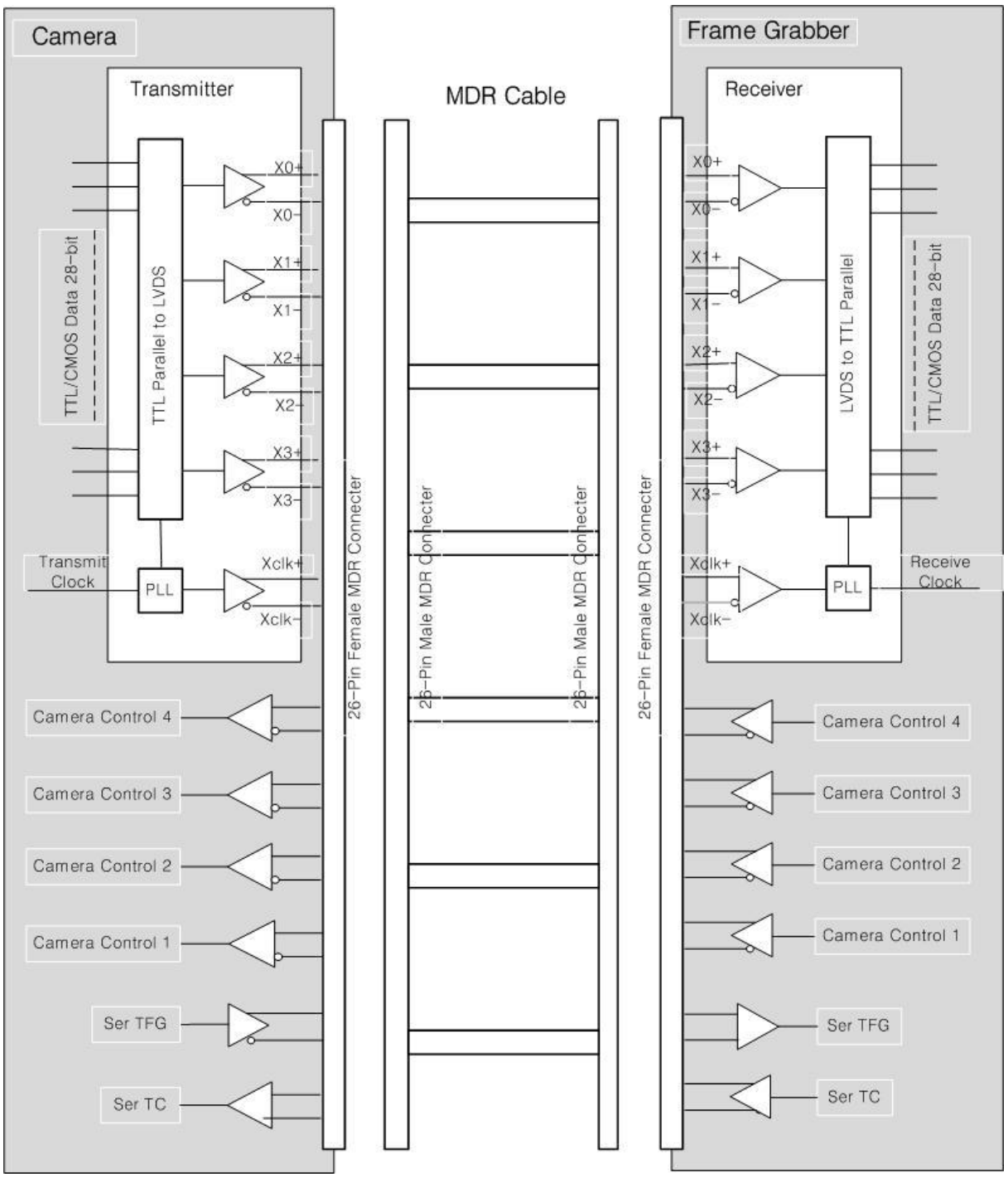
2-2 Camera Link

Camera Link is a communication interface developed for use in vision applications. In the past, we used proprietary connectors and cables between camera makers and frame grabber makers. This caused a lot of confusion and cost increase for users. In order to resolve this confusion, increasing data rate, and confusion in data transmission, the specifications of the Camera Link interface are the specifications of cable or connector assembly, transmission speed and It was made with regulations such as transmission method.

Many digital video solutions today use Low Voltage Differential Signal (LVDS) communication defined by RS-644. RS-644 LVDS has become the Camera Link standard by improving the existing RS-422 method, which had inconvenient cables and limited transmission speed. LVDS can transmit data at high speed by using a differential signal with a low voltage swing. Compared to the existing single-ended signal using one line, the differential signal transmits the signal using two complementary lines. This transmission structure has the characteristics of large-scale common-phase voltage rejection, low power consumption, and excellent noise immunity, which is impossible with single-ended systems that only reference ground for data transmission.

An advanced LVDS technology for the transmission of digital data is a Channel Link. The channel link can transmit parallel-to-serial and serial-to-parallel at 2.38 Gbps. Referring to Figure 2-3, the transmitter converts 28-bit CMOS/TTL data into 4 LVDS data streams. The converted signal is transmitted to the MDR cable according to the Transmit Clock, and the opposite receiver converts these four LVDS data into a 28-bit CMOS/TTL parallel signal according to the Receive Clock. This channel link technology is being used as a low-cost chipset that is easy to learn and portable, so that it can be used immediately.

Camera Link interface includes Base Configuration, Medium Configuration, and Full Configuration. Base Configuration uses four RS-644 LVDS pairs for transmitter/receiver and camera control as shown in Figure 2-3, and uses two RS-644 LVDS pairs for communication between camera and frame grabber. The data transmitted serially through the 26-Pin MDR Cable is changed to 28-bit parallel image data at the Receive end of the frame grabber and used.

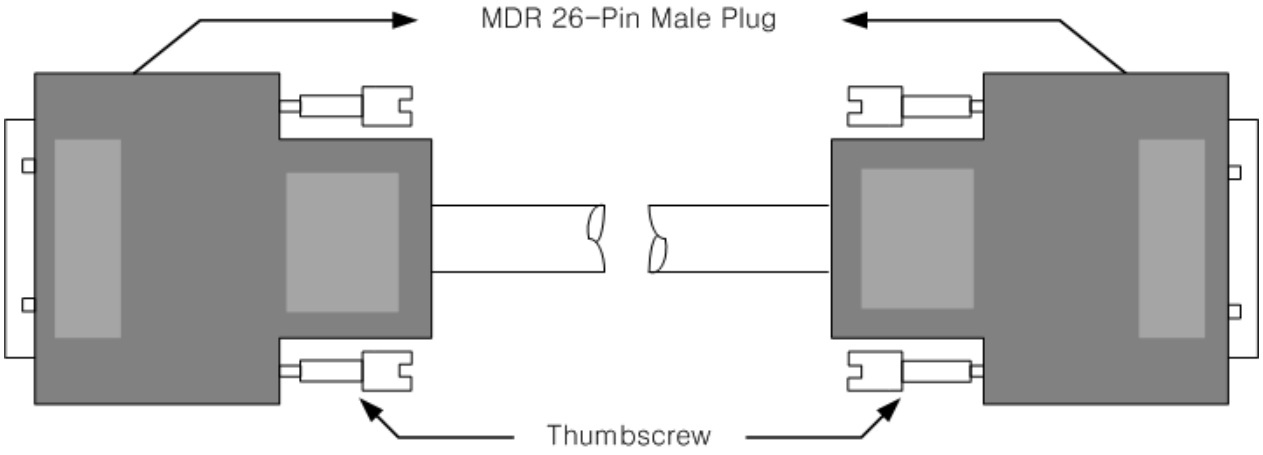


[Figure 2-2. Base Camera Link Block Diagram]

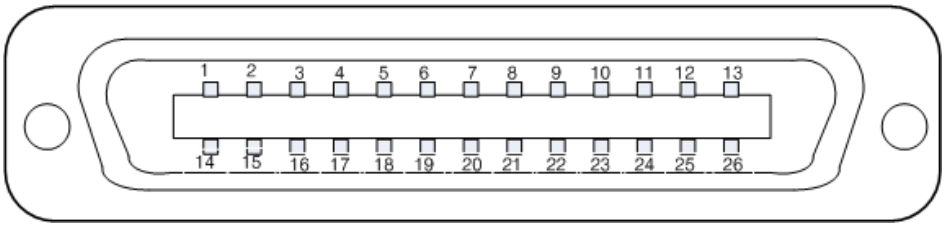
2-3 Camera Link Cable & Connector

Camera Link The connection between the camera and the cPCI-FRM11 board uses a 26 Pin MDR (Mini D Ribbon) cable. The camera link cable consists of a twin-axial shielded cable and two MDR 26-male plugs. [Figure 2-3] below is a commonly used camera link cable.

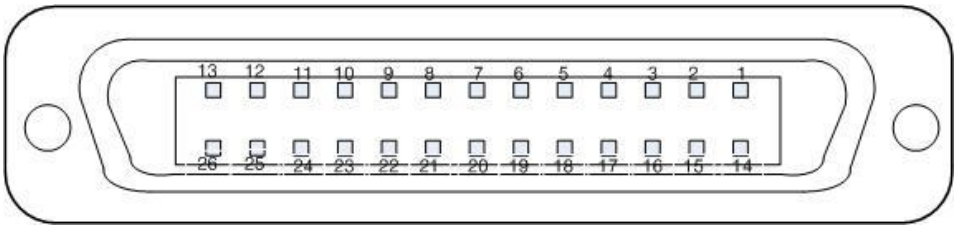
[Figure 2-4] is a 26-Pin Male MDR Connecter located at both ends of the cable, and [Figure 2-5] is a 26-Pin Female MDR Connector, located at the camera or frame grabber. As shown in the figure, the pin numbers are cross-connected, so that the transmitter and receiver terminals of the camera and frame grabber signal lines are cross-connected.



[Figure 2-3. MDR-26 Camera Link Straight Cable]



[Figure 2-4. MDR-26 Cable Pin Map]

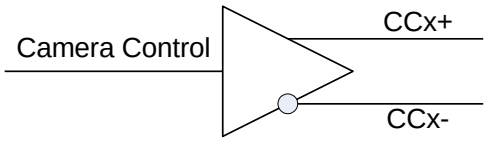


[Figure 2-5. MDR-26 Connector Pin Map (Opposite Connector)]

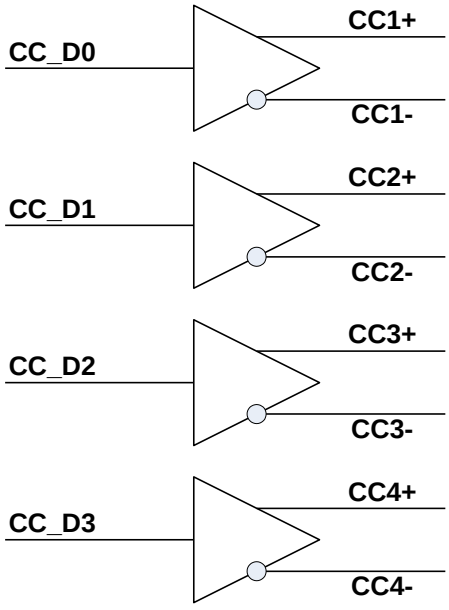
2-5 Camera Link & cPCI-FRM11

cPCI-FRM11 supports Camera Link Base Configuration. Base Configuration consists of 4 LVDS signal lines serializing 28-bit parallel signals including 24 data bits and 4 enable signals Frame Valid, Line Valid, Data Valid, and a spare, and 1 LVDS signal line to synchronize with the camera. , Asynchronous serial communication including 4 CC (Camera Control) signals and 2 LVDS lines for asynchronous serial communication to communicate with the camera are transmitted through MDR cables.

The transmitted signal deserilizes 4 video LVDS serial signals into 28-bit parallel video signals and control signals (Frame Valid, Line Valid, Data Valid, and a spare) through the Channel Link chip in cPCI-FRM11. In addition, a clock signal is made with one LVDS to synchronize the signal between the camera and cPCI-FRM11, and the remaining cameras control signals and communication signals are converted into general TTL signal levels and used.

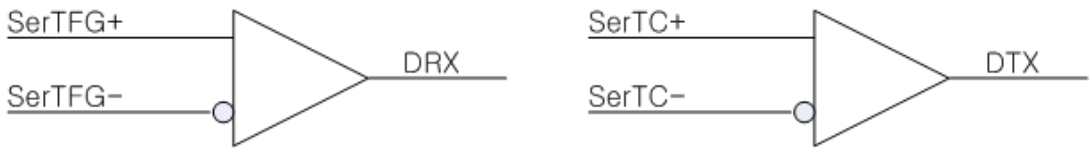


The figure shows the Camera Control output circuit that can send the control signal from the cPCI-FRM11 board to the Camera through the Camera-link cable. A total of 4 digital outputs are output through the differential method. Each output is mapped to a digital output and becomes an output. Each bit position is shown in [Figure 2-6] below.



[Figure 2-6. Camera Control LVDS Digital Output Circuit]

The figure below shows the circuit that uses the serial input signal input through the Camera-link cable as a general input on the cPCI-FRM11 board.



[Figure 2-7. Serial Communication LVDS Digital Output Circuit]

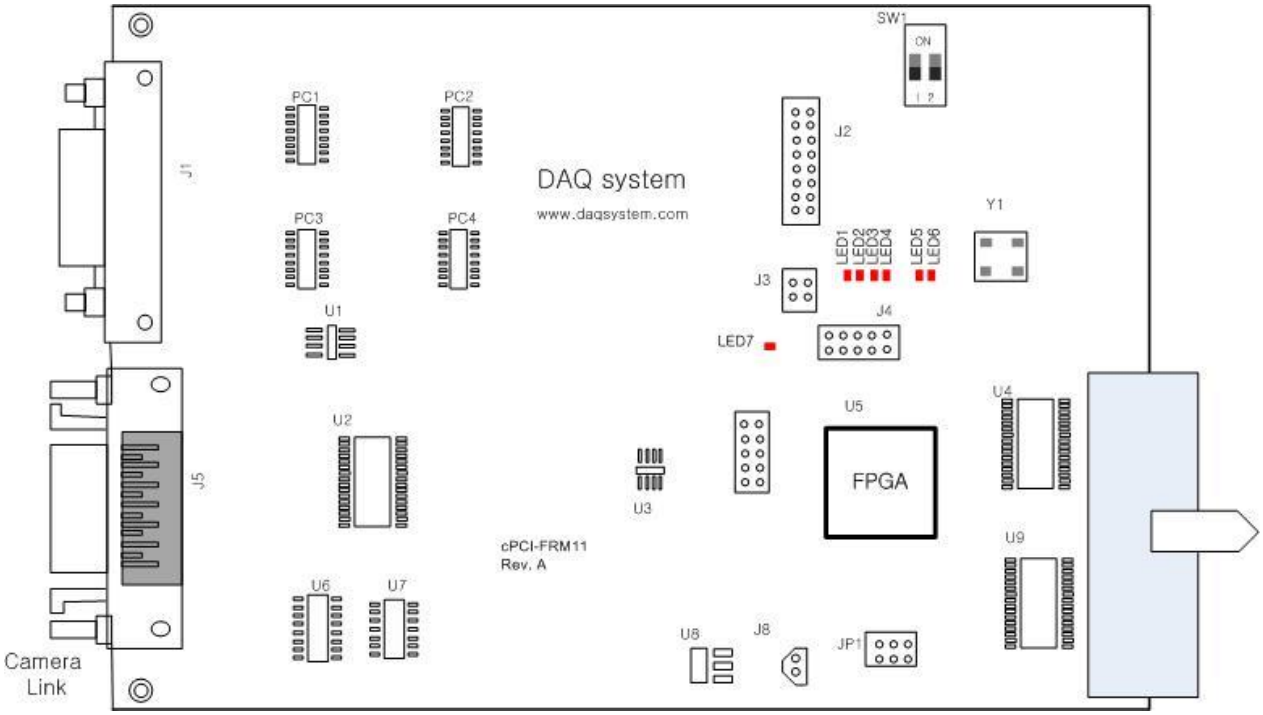
cPCI-FRM11 supports Base Configuration including the following bit allocation.

- 1, 2 ,or 3 Pixels (or Taps) at 8 Bits
- 1 or 2 Pixels (or Taps) at 10 Bits
- 1 or 2 Pixels (or Taps) at 12 Bits
- 1 Pixel (or Tap) at 14 Bits
- 1 Pixel (or Tap) at 16 Bits
- 24 Bits RGB

3. cPCI-FRM11 Board Description

In this chapter, the primary functions of the cPCI-FRM11 board are described briefly. For more information, refer to the device specification.

3-1 cPCI-FRM11 Board Layout



[Figure 3-1. cPCI-FRM11 Layout]

The board has seven LEDs to indicate the operation status.

- LED7 turns on when power is applied to the board and the initialization ends up.
- LED6 turns on when the board receives the image frame data via Camera Link.
- LED5 turns on when the board transmits the received data to your PC.
- LED4..1 : Indicators (turns on always currently.)

3-2 Device Features

(1) **FPGA : U5**

All of the board functions are controlled by the Logic program of the FPGA.

(2) **LVDS : U4, U9**

Receive Image frame through LVDS interface.

UART signal Receive/Transmit through LVDS interface.

Camera Control Digital Output.

(3) **Regulator : U6**

This block is for supplying the power to the board

(4) **Level Shifter : U2**

It is protected a circuit that the interface of high voltage higher than 3.3V CMOS Logic is exchanged to normal 3.3V Logic Level.

(5) **SW1**

It set a board number.

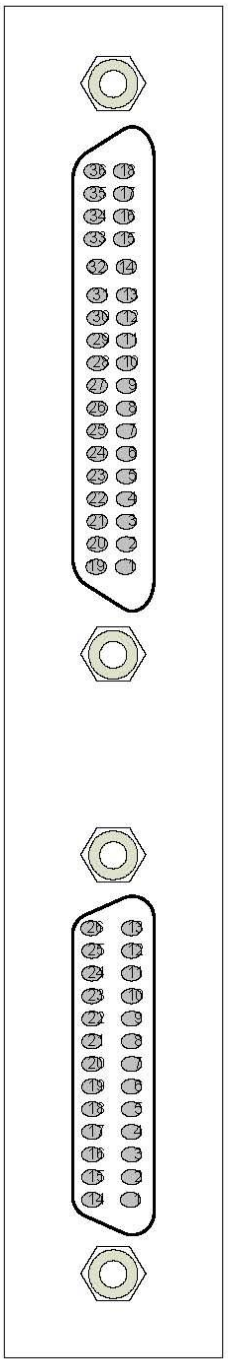
(6) **Photo-coupler Isolated I/O : PC1 ~ PC4**

This block is for controlling isolated digital I/O circuit with external device.

3-3 Connector Pin-out

This section describes the connectors and jumpers used in cPCI-FRM11. As for main connectors, there are MDR 26pin connector for Camera Link connection and MDR 36pin connector for external digital input/output connection port.

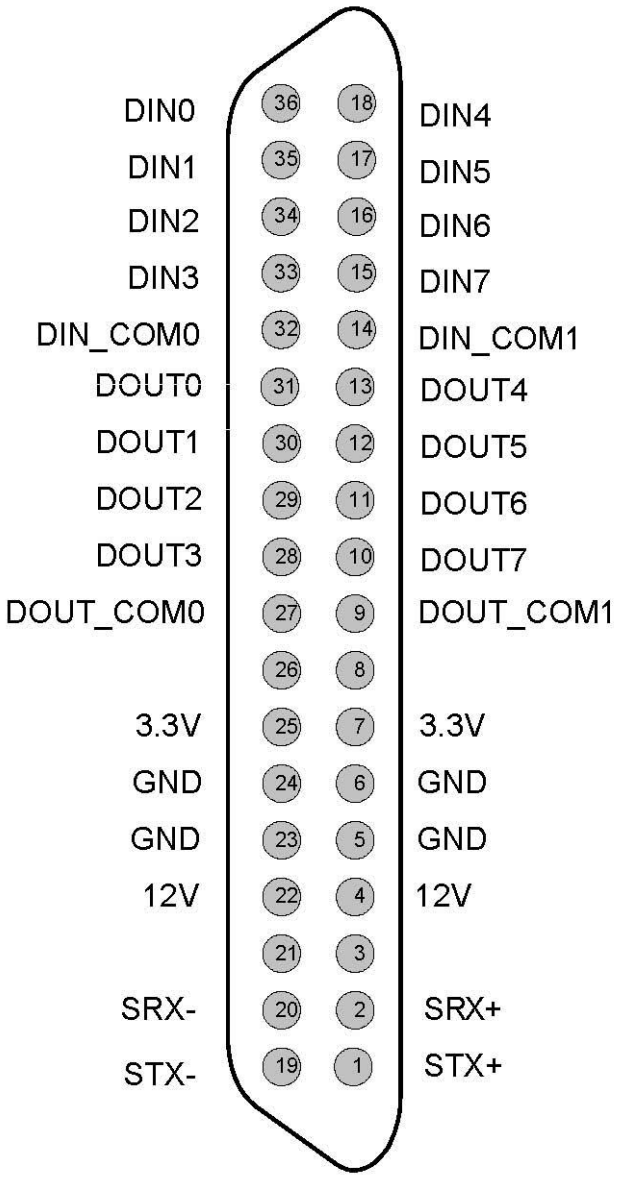
[Figure 3-2] shows the bracket that interfaces with the board and the outside, and the connection connector.



[Figure 3-2. cPCI-FRM11 Front View]

3-3-1 J1 (MDR36) Connector

[Table 1] below shows the pin map of the J1 (MDR36) connector of the board.

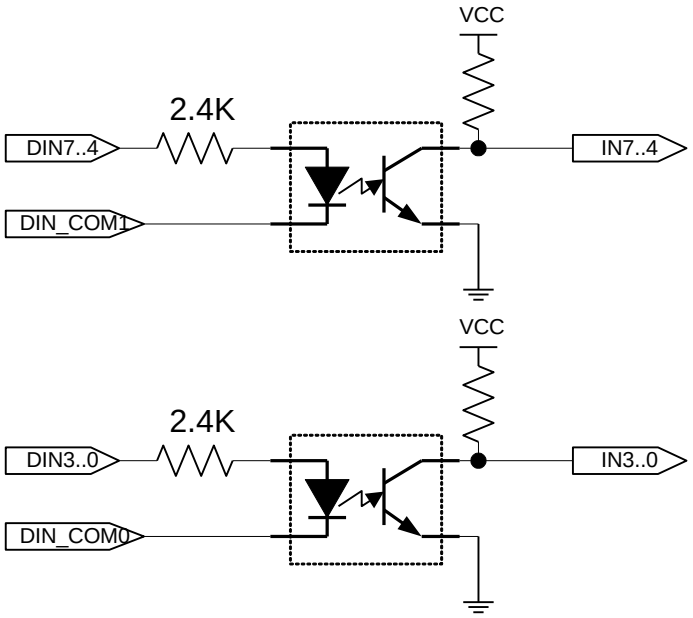


[Figure 3-3. cPCI-FRM11 J1 Connector Pin-out]

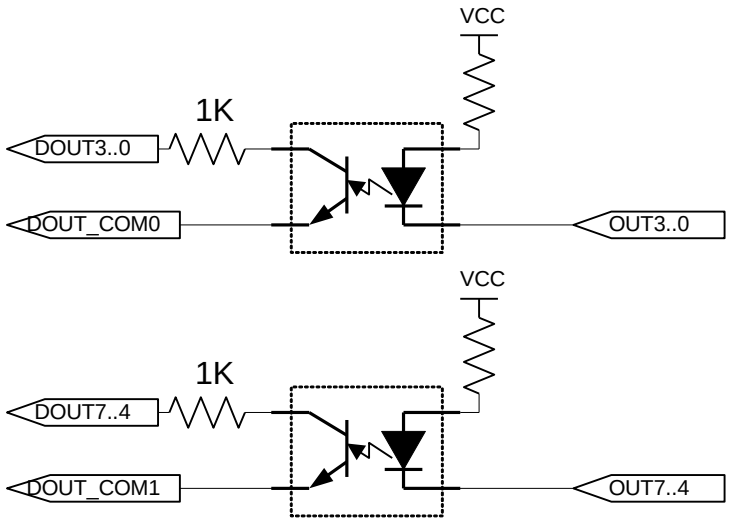
[Table 1. J1 Connector]

Pin No.	Name	Description
1	**STX+**	LINE TRIGGER OUT+
2	**SRX+**	LINE TRIGGER IN+
3	**-**	
4	**+12V**	+12V
5	**GND**	GND
6	**GND**	GND
7	**3.3V**	3.3V
8	**-**	
9	**DOUT_COM1**	OUTPUT COMMON 1 (FOR output 4,5,6,7)
10	**DOUT**	OUTPUT 7
11	**DOUT**	OUTPUT 6
12	**DOUT**	OUTPUT 5
13	**DOUT**	OUTPUT 4
14	**DIN**	INPUT COMMON1 (FOR input 4,5,6,7)
15	**DIN**	INPUT 7
16	**DIN**	INPUT 6
17	**DIN**	INPUT 5
18	**DIN**	INPUT 4
19	**STX-**	LINE TRIGGER OUT-
20	**SRX-**	LINE TRIGGER IN-
21	**-**	
22	**+12V**	+12V
23	**GND**	GND
24	**GND**	GND
25	**3.3V**	3.3V
26	**-**	
27	**DOUT_COM0**	OUTPUT COMMON0 (FOR output 0,1,2,3)
28	**DOUT3**	OUTPUT 3
29	**DOUT2**	OUTPUT 2
30	**DOUT1**	OUTPUT 1
31	**DOUT0**	OUTPUT 0
32	**DIN_COM0**	INPUT COMMON0 (FOR input 0,1,2,3)
33	**DIN3**	INPUT 3
34	**DIN2**	INPUT 2
35	**DIN1**	INPUT 1
36	**DIN0**	INPUT 0

In cPCI-FRM11 board, 8 digital inputs and 8 digital outputs isolated by photo-couplers can be used through J1 connector. The circuit is shown in [Figure 3-4].



< Photo coupler input>



<Photo coupler output>

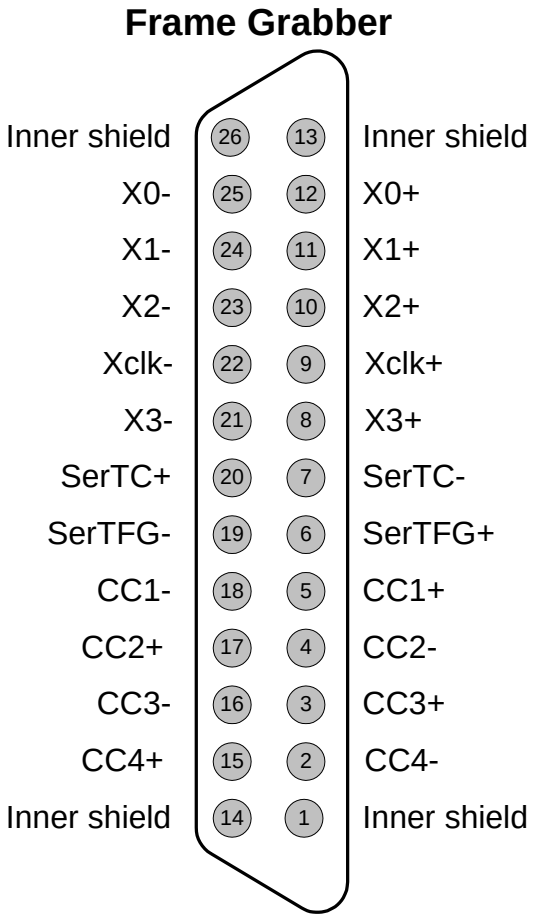
[Figure 3-4. Photo-coupler Input/ Output circuit]

For input, using a resistance of 2.4KΩ (Ohm), about 5mA for 12V input and about 10mA for 24V input will flow. Available input voltage is within 9V to 24V.

The output uses a 1KΩ (ohm) resistor to limit the maximum output current. Output current should be used within 5mA. In special circumstances, the R value is adjusted and used to operate according to the above description.

3-3-2 J5 (MDR26) Connector

The figure below shows the pin map of the J5 connector of the board used when using the Base Configuration Camera Link. All pin specifications are input/output based on the Camera Link standard, so please refer to the Camera Link standard document for details.



[Figure 3-5. cPCI-FRM11 J5 Connector Pin-out]

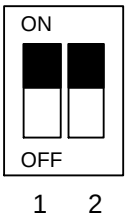
[Table 1. J5 Connector]

Pin No.	Name	Description	Remark
1	**Inner Shield**	Cable shield	
2	**CC4-**	Camera Control output 4-	
3	**CC3+**	Camera Control output 3+	
4	**CC2--**	Camera Control output 2-	
5	**CC1+**	Camera Control output 1+	
6	**SerTFG+**	Serial to Frame grabber +	
7	**SerTC-**	Serial to Camera-	
8	**X3+**	Camera link LVDS receive data3 +	
9	**Xclk+**	Camera link LVDS receive clock +	
10	**X2+**	Camera link LVDS receive data2 +	
11	**X1+**	Camera link LVDS receive data1 +	
12	**X0+**	Camera link LVDS receive data0 +	
13	**Inner Shield**		
14	**Inner Shield**		
15	**CC4+**	Camera Control output 4+	
16	**CC3-**	Camera Control output 3-	
17	**CC2+**	Camera Control output 2+	
18	**CC1-**	Camera Control output 1-	
19	**SerTFG-**	Serial to Frame grabber-	
20	**SerTC+**	Serial to Camera+	
21	**X3-**	Camera link LVDS receive data3-	
22	**Xclk-**	Camera link LVDS receive clock-	
23	**X2-**	Camera link LVDS receive data2-	
24	**X1-**	Camera link LVDS receive data1-	
25	**X0-**	Camera link LVDS receive data0-	
26	**Inner Shield**		

(Note) For detailed specifications, refer to the Camera Link standard document.

3-3-3 SW1 Switch

cPCI-FRM11 board is designed to use up to 4 cPCI-FRM11 boards simultaneously in one system (PC). Each board classification can be set through the 4-pin DIP switch in the board.



[Figure 3-6. SW1 Switch (Top View)]

[Table 4. SW1 PIN-OUT]

1	2	Description
OFF	**OFF**	Board No. 0
ON	**OFF**	Board No. 1
OFF	**ON**	Board No. 2
ON	**ON**	Board No. 3

3-3-4 J4 Connector

It is a 3.3V external DC power connector. This is the power used when installing the FPGA and is not normally used.

3-3-5 JP3 Connector

JP3 is a JTAG (Joint Test Action Group) connector and is used to update the FPGA program on the board. Do not use when operating the board normally.

4. Installation

4-1 Product Contents

Before installing the board, check that the contents of the package are intact.

1. cPCI-FRM11 Board
2. CD (Drivers/Manual/API/Sample source etc.)

4-2 Installation Process

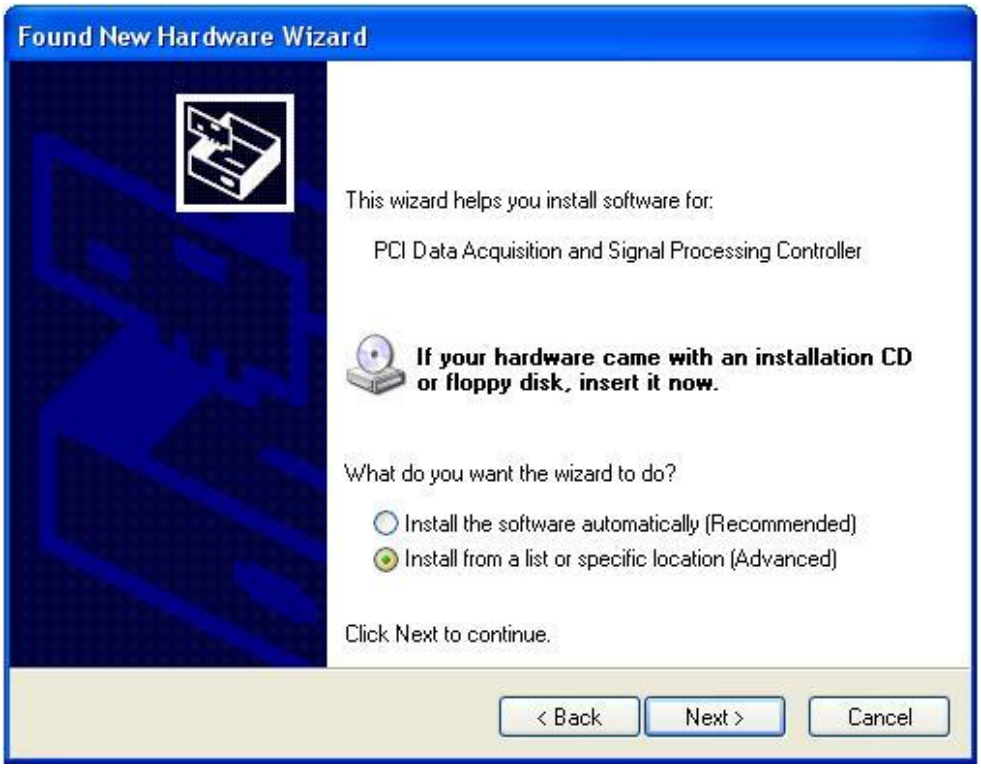
① Turn off the computer.
② Remove the computer cover according to the computer manual.
③ After removing the blocked part at the back of the computer case in the slot where the board is inserted, tightly fasten the screws between the bracket of the board and the case.
④ In case of multi-board, repeat from step 2.
⑤ When the power is off, plug the cPCI-FTM11 board into the PCI SLOT and apply power, LED3 turns on, and LEDs 1 and 2 repeat On/Off.

After installing the board, install the driver and sample application to run the board on your PC. For installation, use the supplied CD.

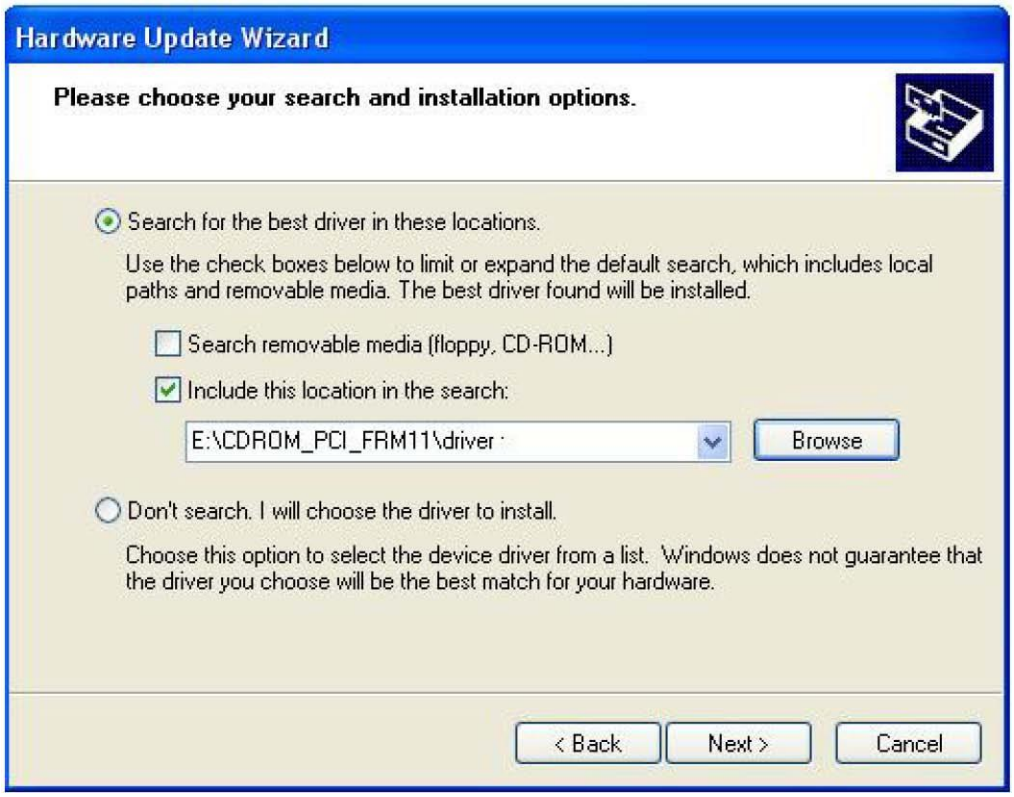
The installation procedure is as follows, and unless otherwise specified, it is explained based on Windows XP.

The board environment must be Windows 2000 SP4 or higher and Windows XP SP1 or higher. First, turn off the PC's power, plug the cPCI-FRM11 board into the Compact PCI Slot, and turn on the PC's power. When the "Start New Hardware Wizard" window opens as shown below, selects it as shown below and click the Next button.

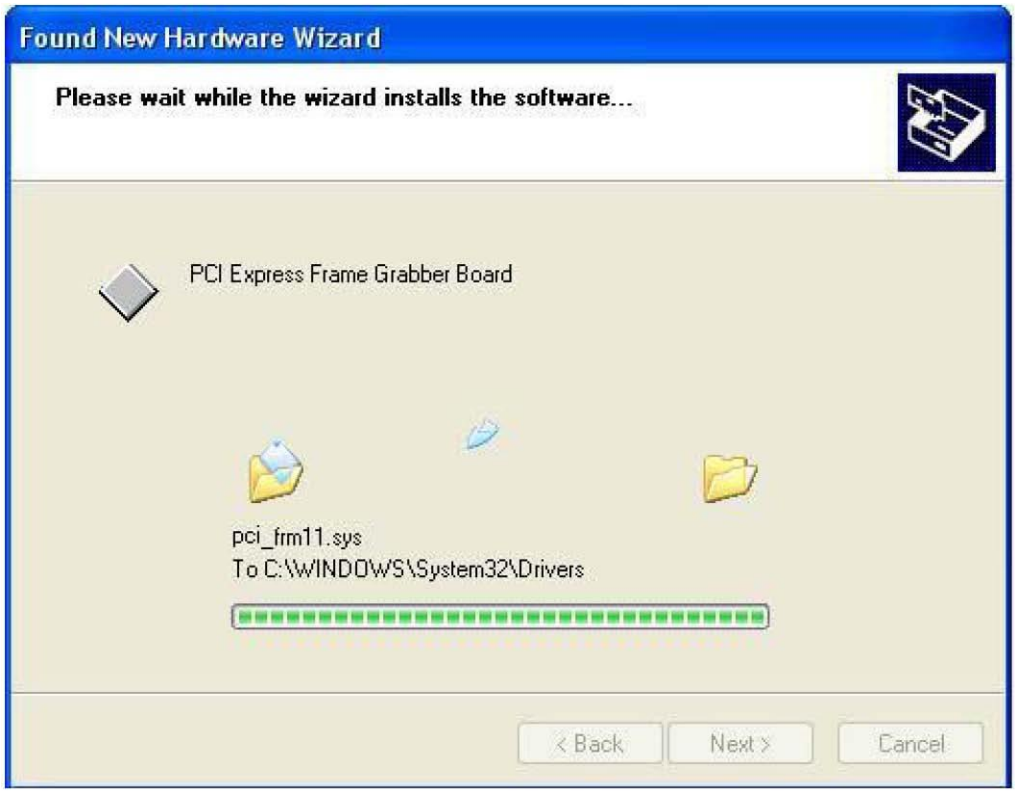
1. Select as below and click the Next button



2. Select Driver from the enclosed CD and click the Next button.



3. Click the Next button. It indicates that the installation process is proceeding as shown below. The driver folder contains **"pci_frm11.inf"** and **"pci_frm11.sys"** files required for driver installation. Click Next to install the driver files.

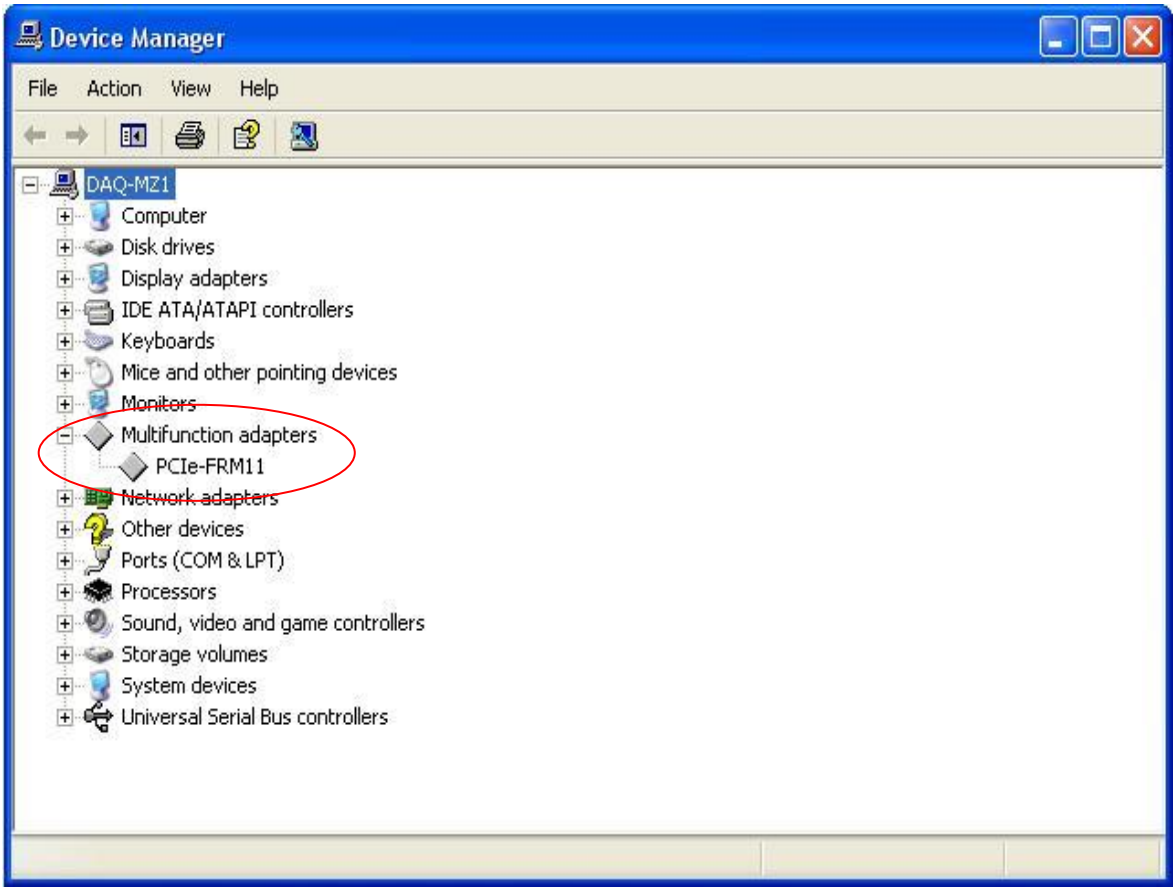


4. When the installation is completed normally, it is shown in the figure below.

5. When the installation is complete, check whether the driver is installed normally in the following way.

6. In My Computer -> Properties -> Hardware -> Device Manager, check if the **Multifunction Adapter -> "PCIe-FRM11"** is installed.

7. If it appears as shown in the figure below, the installation has been completed normally.



The above figure shows the screen where the cPCI-FRM11 board is normally installed in the PC.

(Note) cPCI-FRM11 board is registered as a PCIe-FRM11 device to maintain compatibility with the existing PCIe-FRM11 board.

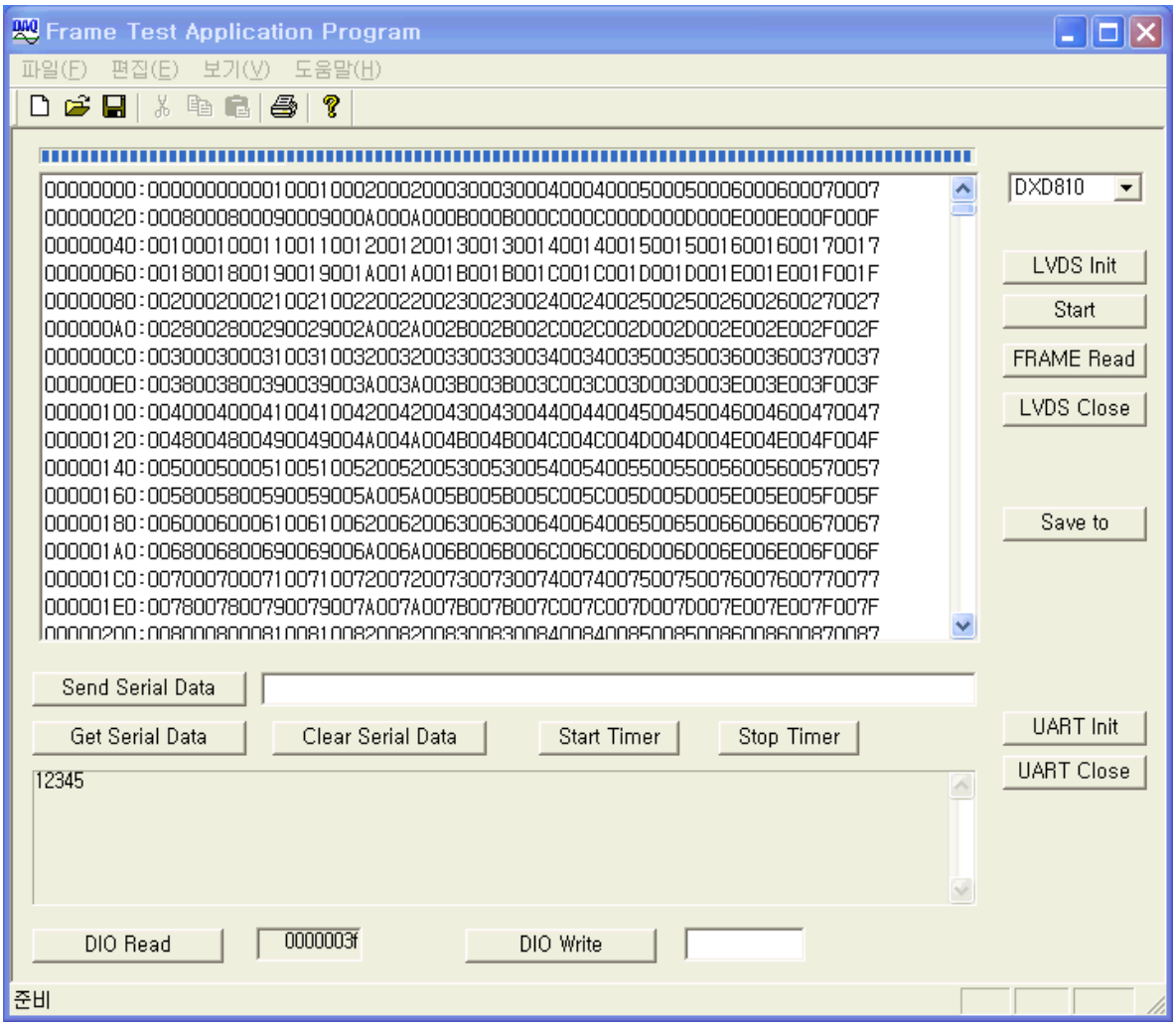
(Note) After initial installation, the PC must be rebooted for normal operation.

5. Sample Program

In the CDROM folder provided with the board, a sample program is provided for easy use of the board. First of all**, "FrmTest.exe",** one of the executable files, displays Frame Data as a hexadecimal value and stores it in memory or hard disk so that developers can utilize the necessary frame data.

In order to test the sample program, the driver of the board must be installed first. The sample program is provided in source form so that the API provided to use the board can be tested briefly, so the user can modify it and use it.

5-1 FrmTest Program



[Figure 5-1. Sample Program "FrmTest.exe"]

API (Application Programming Interface) is required to use the above sample program. API is provided in the form of "DLL", and import library and header file are required to compile. All files specified above are included on the supplied CDROM. In order to run the sample program normally, the API DLL (pci_frm11.dll) must be in the folder of the executable file or in the Windows system

folder or the folder specified by the Path environment variable.

5-1-1 Image Frame Function

(1) '**DXD810/DXD1417' Combo-box**

Use this box to set up the operation mode.

(2) '**LVDS Init' button**

Press this button to initialize the function of receiving image frame data. It is performed only once after power is applied to the board.

(3) '**Start' button**

Press this button to begin to save image data from Camera Link.

(4) '**FRAME Read' button**

Press this button to read the image frame data of the board to your PC. If image frame data is not saved on the board, you must wait until the end of data collection.

(5) '**LVDS Close' button**

Press this button to finish usage of the board and terminate the program.

(6) '**Save to' button**

Press this button to save the image frame data.

5-1-2 UART Function

(1) '**Send Serial Data' button**

Press this button to send the data in the editor box to UART. You can directly write the data in the editor box by the button.

(2) '**Get Serial Data' button**

Press this button to get the data on the general UART.

(3) '**Clear Serial Data' button**

Press this button to clear the contents of the editor box.

(4) '**Start Timer' button**

Press this button to start the timer. The sample program will read the UART data periodically. The reading interval is around 0.1s.

(5) '**Stop Timer' button**

Press this button to stop the timer.

(6) '**UART Init' button**

Press this button to initialize UART. It must be performed only once after power is applied to the board.

(7) '**UART Close' button**

Press this button to finish usage of the board and terminate the program.

5-1-3 DIO Function

(1) '**DIO Read' button**

Press this button to read the data on General Purpose I/O port. It will be written an editor box.

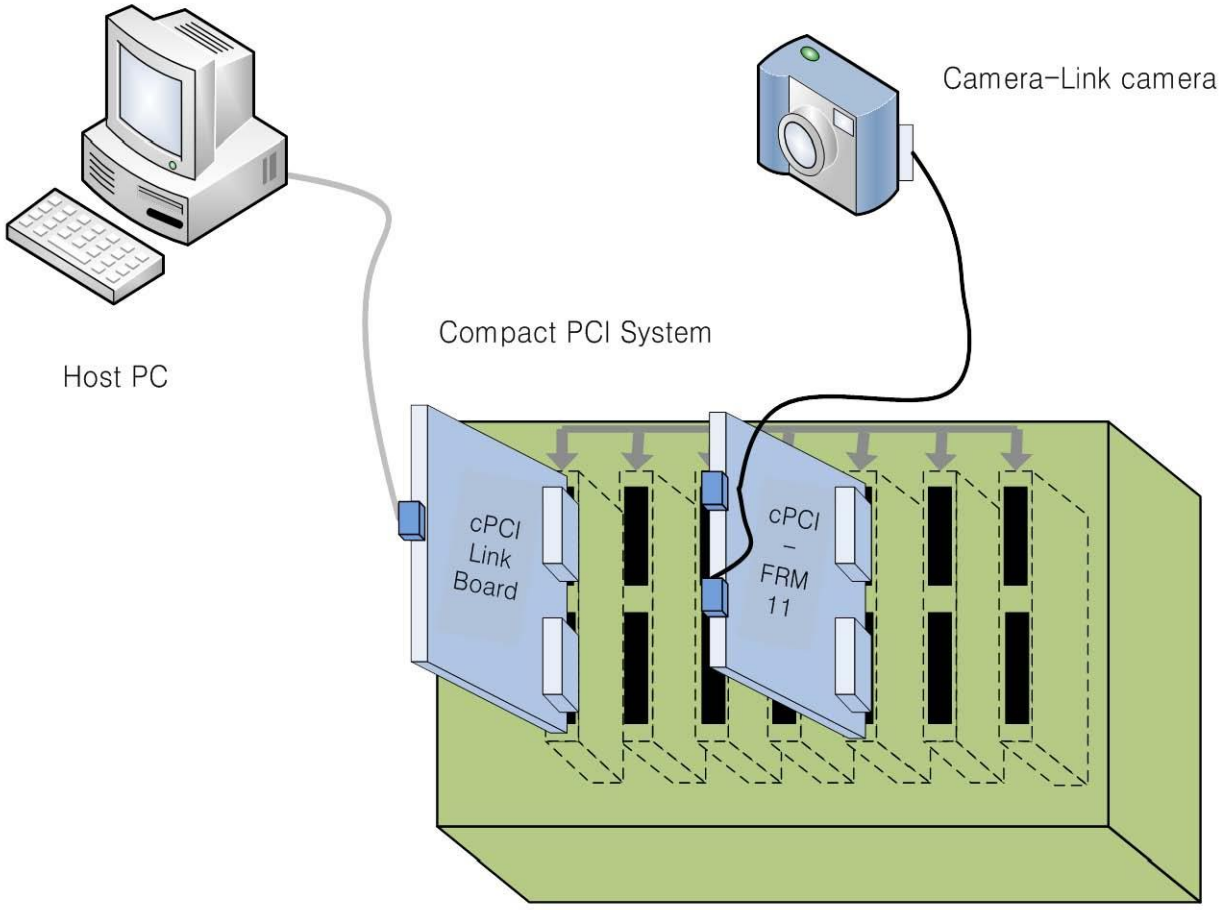
(2) '**DIO Write' button**

Press this button to write the data on General Purpose I/O port. You can directly write the data in the editor box beside the button.

6. Test

6-1 Image Frame Input Test

In this chapter, the functional test will be explained to discriminate board mal-functions and for the user being familiar with the operation of the board. It is performed using the sample program **"FrmTest.exe"**.



[Figure 6-1. Equipment Connection for Testing]

In the figure above, the cPCI-FRM11 board is installed in the PC, but the figure is drawn outside for better understanding. The image frame simulator uses a self-made one by the DAQ system, and if you have an actual device, you can use it.

Complete the wiring as shown in the figure above and apply power. After confirming that the cPCI-FRM11 board is registered in the PC, run the sample program ("FrmTest.exe") on the PC.

(1) After initializing by pressing the "LVDS init" button, click the "Start" button to save the image frame.

(2) Press the "Frame Read" button to load the image data of the program. The read data is displayed in the editor box, so check whether it matches the actual data sent. In some cases, a separate verification program must be used, so press the "**Save to"** button to save the read data as a file and check whether there is any abnormality in the data.

6-2 UART Tx/Rx Test

In the above connection state, the image frame simulator periodically transmits serial data to the board.

(1) After initialization by pressing the UART init button, press the "Start Timer" button to periodically read the UART data transmitted from the simulator and display it on the screen.

(2) As shown in [Figure 5-1], write the character you want to send in the editor box next to the "Send Serial Data" button and press the button to transmit the UART data. The transmitted data is checked in the simulator.

6-3 DIO Test

Continue the test in the above connection condition.

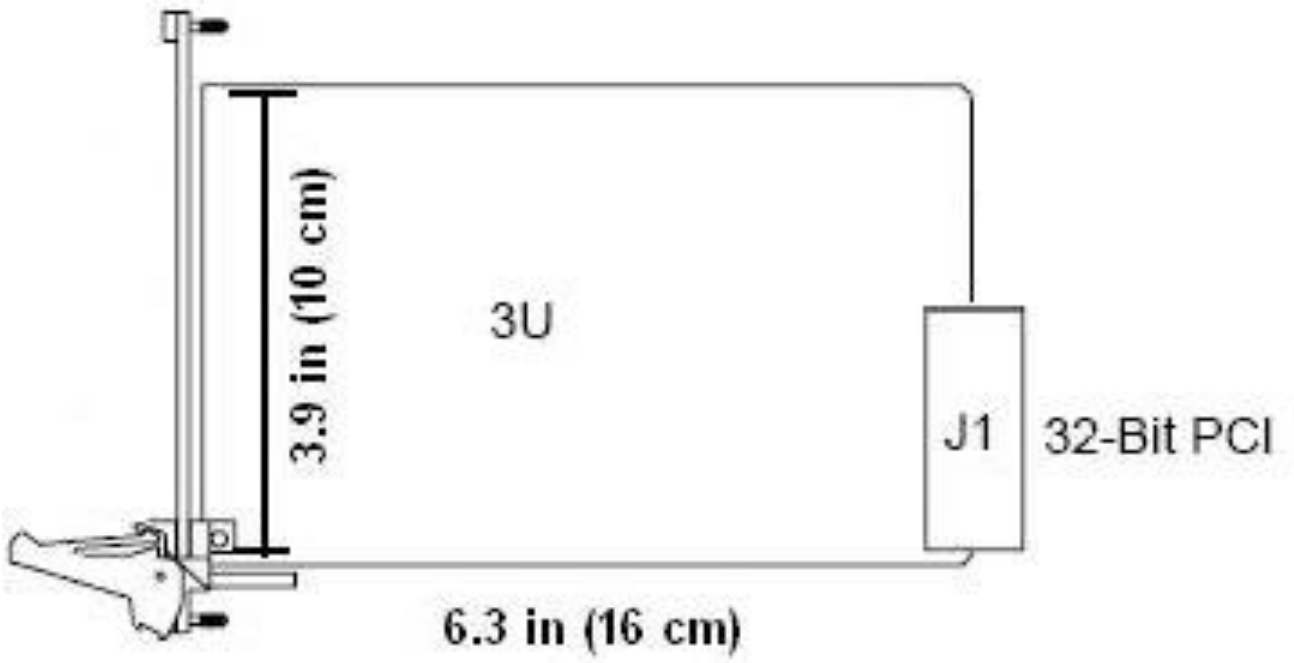
(1) Make sure that all output ports are "1" with "DIO Write" function and check with the oscilloscope. In order to check the LVDS output and the photo-coupler output with an oscilloscope, an external circuit configuration is required.

(2) Check the input with "DIO Read" function. At this time, test the photo-coupler and a separate external circuit for LVDS input.

Appendix

A-1 Board Size

The external sizes of the board are as follows.
For detailed dimensions, please contact the person in charge.



A-2 Repair Regulations

Thank you for purchasing a DAQ SYSTEM product. Please refer to the following regarding Customer Service regulated by DAQ SYSTEM.

(1) Read the user manual and follow the instructions before using the DAQ SYSTEM product.

(2) When returning the product to be repaired, please write down the symptoms of the failure and send it to the head office.

(3) All DAQ SYSTEM products have a 1-year warranty.
- -. Warranty period counts from the date the product is shipped from DAQ SYSTEM.
- -. Peripherals and third-party products not manufactured by DAQ SYSTEM are covered by the manufacturer's warranty.
- -. If you need repairs, please contact the Contact Point below..

(4) Even during the warranty period, repairs are charged in the following cases..
- ① Failure or damage caused by use without following the user's manual
- ② Failure or damage caused by customer's negligence during product transportation after purchase
- ③ Failure or damage caused by natural phenomena such as fire, earthquake, flood, lightning, pollution, or power supply exceeding the recommended range
- ④ Failure or damage caused by inappropriate storage environment (e.g. high temperature, high humidity, volatile chemicals, etc.)
- ⑤ Breakdown or damage due to unreasonable repair or modification
- ⑥ Products whose serial number has been changed or removed intentionally
- ⑦ If DAQ SYSTEM determines that it is the customer's fault for other reasons

(5) Shipping costs for returning the repaired product to DAQ SYSTEM are the responsibility of the customer.

(6) The manufacturer is not responsible for any problems caused by misuse, regardless of our warranty terms.

References

1. Specification of Camera Link Interface Standard for Digital Cameras and Frame Grabbers
-- Camera Link committee
2. PCI Local Bus Specification Revision2.1
-- PCI Special Interest Group
3. AN201 How to build application using API
-- DAQ system
4. AN312 PCIeFRM11 API Programming
-- DAQ system

MEMO

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