USB-IK01

User Manual

Version 1.0

DAQ SYSTEM
Measurement & Automation

Contents

1. Introduction ---------- 2

2. USB-IK01 Features ---------- 3

3. USB-IK01 Board Description

3-1 USB-IK01 Concept ---------- 4
3-2 Product Contents ---------- 5
3-3 Memory Map ---------- 6

4. EPLD(XC9536XL) Program

4-1 VHDL Sample Source ---------- 8
4-2 Compiling VHDL using ISE ---------- 10
4-3 Chip programming using ISE ---------- 11

5. Test

5-1 Ready to Test ---------- 12
5-2 PCF8754 Test ---------- 14
5-3 EPLD Test ---------- 15
5-4 RAM Test ---------- 16

Appendix

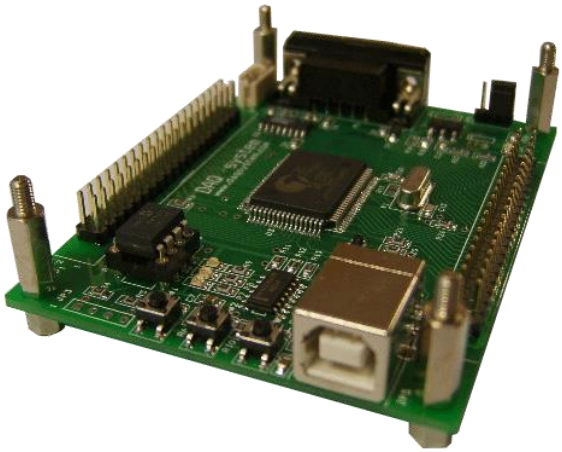
A-1 Board Connector Pin Map ---------- 17
A-2 Repair Regulations ---------- 21

Reference ---------- 22

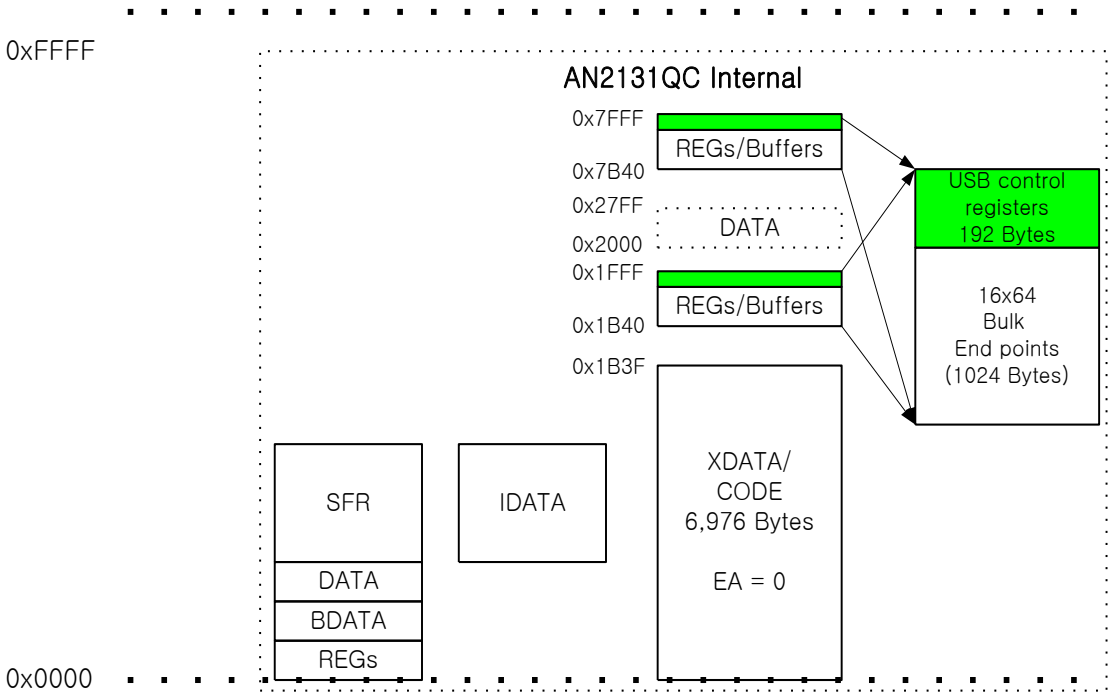
1. Introduction

USB-EK01 is designed as an evaluation board that can perform various tests using minimal memory and I/O (refer to USB-EK01 User's Manual).

Internal 8K Byte memory was sufficient for most tests and applications, but there was a limit to applications requiring large program capacity or large data memory. Therefore, it became necessary to use external memory, and additional I/O expansion and the concept of allowing the user to change the hardware configuration, we designed the USB-IK01 board that can be used by connecting to the external expansion connector of the USB-EK01..



[Figure 1-1. USB-EK01 Layout]



[Figure 1-2. USB-EK01(AN2131) Memory Map]

2. USB-IK01 Features

<Functions>

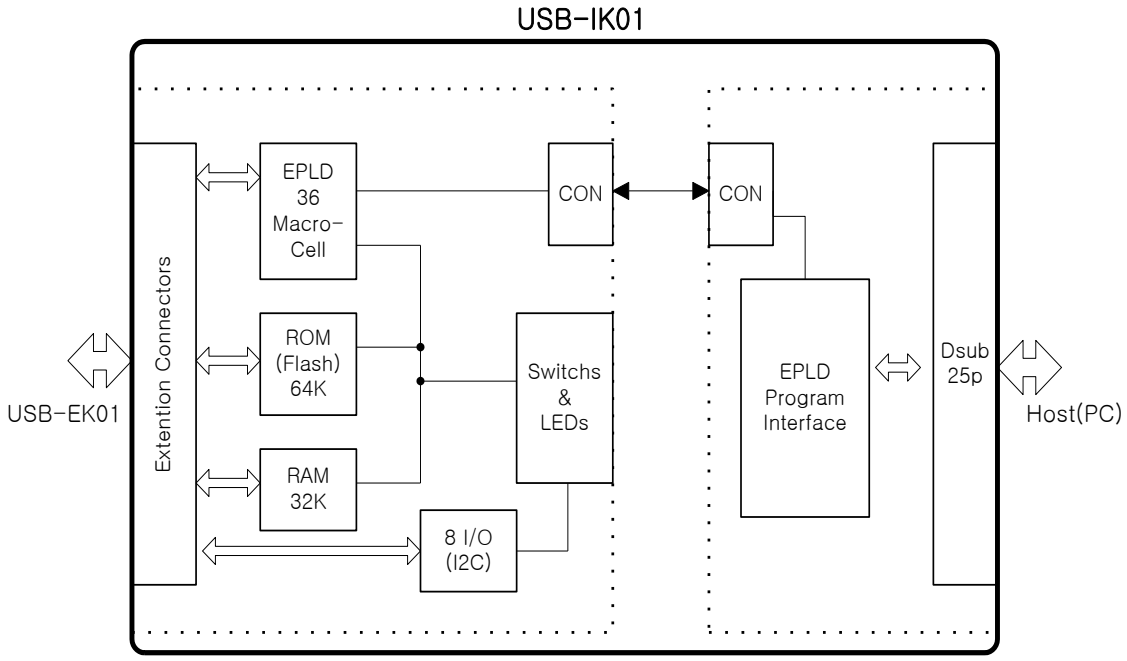
- USB-EK01 function expansion (memory, I/O, etc.)
- XLINX FPGA/EPLD program interface (no separate interface device required)
- Hardware change by EPLD Programming (memory location)
- I/O expansion through EPLD
- I/O expansion through I2C

<Specifications>

- 32K of external RAM
- External ROM (Flash) 64K
- Additional 8 general purpose I/O (I2C serial interface)
- 36 programmable macro cells

3. USB-IK01 Board Description

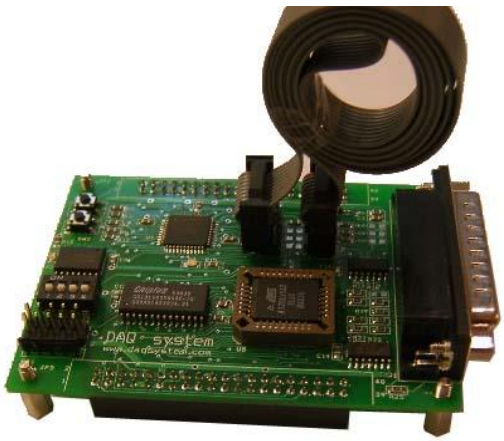
3-1 USB-IK01 Concept



[Figure 3-1. USB-IK01 Function Block Diagram]

The USB-IK01 is largely divided into two parts as indicated by the dotted box (electrically completely separated). First, it is the memory and I/O expansion part using EPLD (XC9536XL), and the interface part that enables the EPLD program itself. Therefore, it is possible to change the hardware configuration without the need for a separate EPLD programmer.

[Figure 3-2. Using USB-IK01 as a programmer]



[Figure 3-3. Self-program connection of EPLD of USB-IK01]

As shown in [Figure 3-2] and [Figure 3-3], the EPLD can be programmed by itself, and it can also be used as a programmer for other boards.

3-2 Product Contents

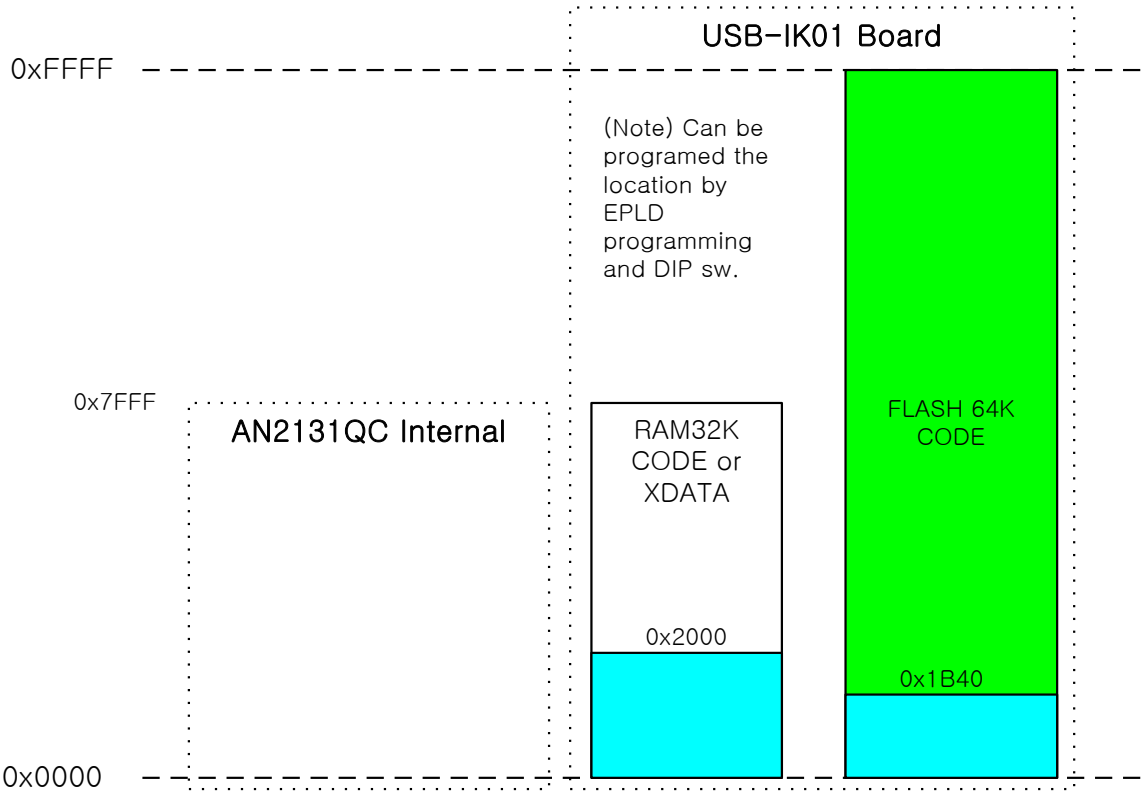
[Figure 3-4. USB-IK01 Main Contents]

(1) USB-IK01 Evaluation board
(2) 25Pin Parallel Cable
(3) 10Pin Flat Cable (EPLD Program)

3-3 Memory Map

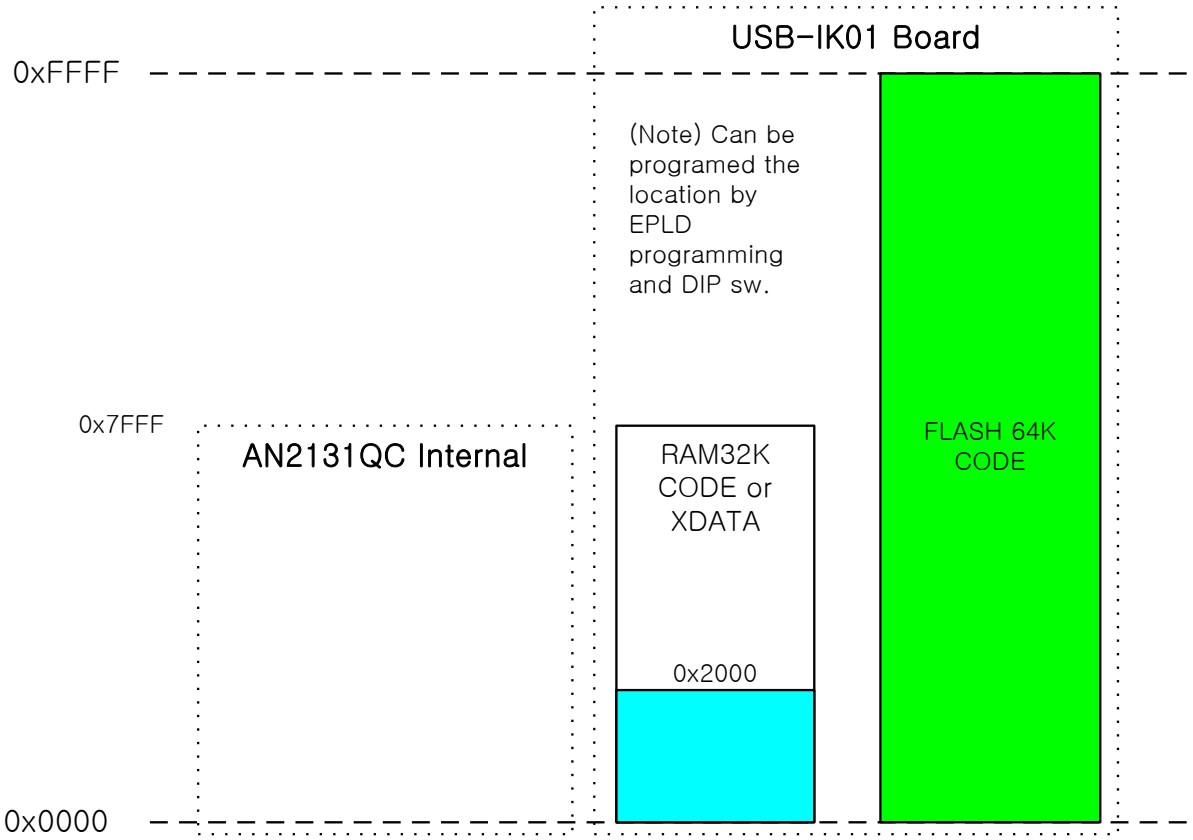
As shown in [Figure 1-2], the memory of USB-EK01 itself is all internal 8K RAM that can be used for data and program at the same time. However, when two boards are connected as shown in [Figure 3-5], 32K RAM and 64K ROM (Flash) installed in USB-IK01 can be used.

[Figure 3-5. USB-IK01 and USB-EK01 combined]



[Figure 3-6. When connection between USB-IK01 and USB-EK01,Memory Map (EA = 0)]

And, depending on the state of the EA pin of the chip, the method of using the program memory is different as in [Figure 3-6] and [Figure 3-7]. made it possible



[Figure 3-7. When connection between USB-IK01 and USB-EK01,Memory Map (EA = 1)]

When the EA pin is High Level '1', the external data memory area is not affected, and the internal RAM of the AN2131 chip can be used as a general data memory.

4. EPLD(XC9536XL) Program

To program the EPLD, combine the two boards as shown in the figure below, connect the printer cable between the PC and USB-IK01, and connect the two connectors in the blue circle shown in the figure to a flat cable as shown in [Figure 4-1]. Connect.

[Figure 4-1. A figure EPLD program of USB-IK01]

4-1 VHLD Sample Source

The VHDL source used can be found in the "Hardware₩USB-IK01" folder of the CDROM provided with the USB-EK01. Below is an excerpt from the VHDL source. Here, MM is defined as "in std_logic_vector(1 downto 0)", is connected to No. 3 and No. 4 of DIP switch, and operates as '0' when ON and '1' when OFF. DIP switch 3 is Bit0.

While analyzing the drawing and the source together, please modify the program source so that it can perform the desired operation.

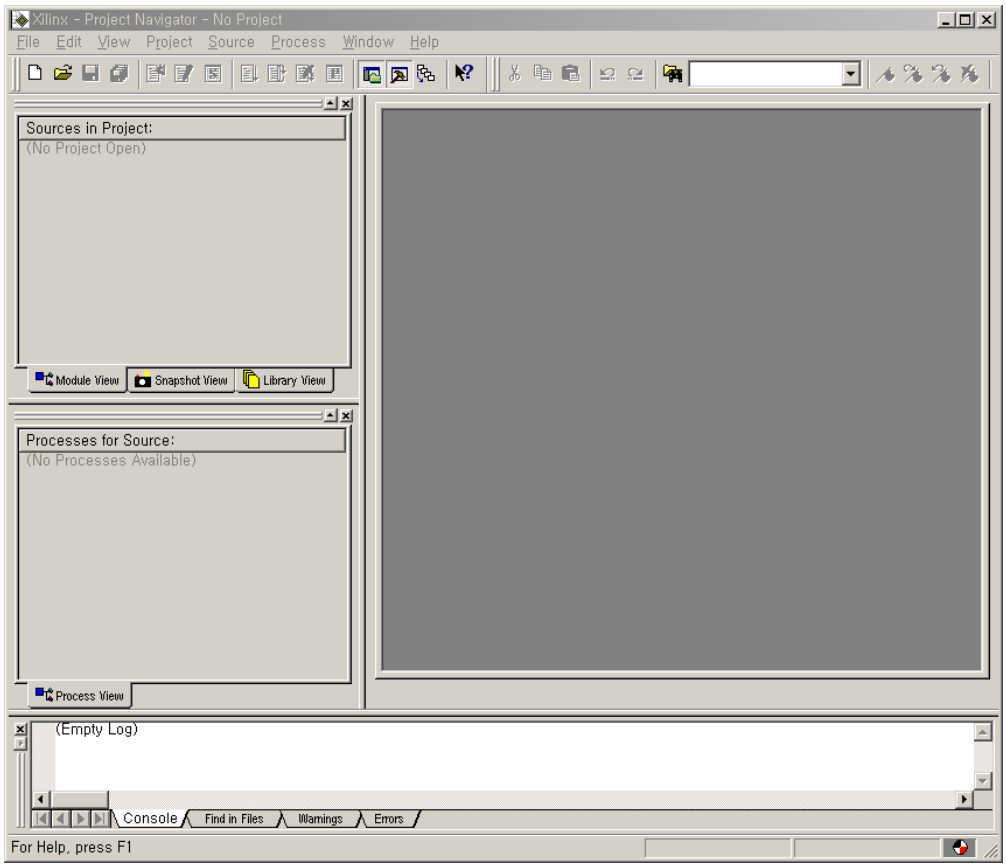
<VHDL Source>

```
decode_prog:process(nRESET,MM)
begin
  if ( nRESET = '0') then
    nCE <= "11";
    nOE <= "11";
    EA   <= '0';
  else
    case MM is
                when "00" =>
              -- No external memory
                          nCE <= "11";
                          nOE <= "11";
                          EA   <= '0';
                when "01" =>
                        -- RAM is located at address 0x8000
                          nCE(2) <= not A(15);
                          nCE(1) <= '1';
                          nOE(2) <= nPSEN and PC(7);
                          nOE(1) <= '1';
                          EA   <= '0';
                when "10" =>
                         -- RAM(0x0)     ROM(0x8000)
                          nCE(2) <= A(15);
                          nCE(1) <= not A(15);
                          nOE(2) <= nPSEN and PC(7);
                          nOE(1) <= nPSEN and PC(7);
                          EA   <= '0';
                when "11" =>
                                                              -- ROM(0x0), RAM(0x8000)
                          nCE(2) <= not A(15);
                          nCE(1) <= A(15);
                          nOE(2) <= nPSEN and PC(7);
                          nOE(1) <= nPSEN and PC(7);
                          EA   <= '1';
                when others => NULL;
      end case;
  end if;
end process;

nWE   <= PC(6);                    -- Write enable
USER <= (others => '0');
SM1   <= BOOT;
nCON <= BOOT;

nPROG      <= PA(0) when PA(1) = '0' else CLK1MHz;

SPARE(1) <= CLK1MHz;

nWAKEUP   <= nINT and nSW_ST;
PA2 <=   nSW_ST;
PA3 <=   nINT;
SPARE(2) <= A(14) and BKPT;
```

4-2 VHDL Compile with using ISE

XC9536XL sold by XILINX was used for the EPLD used in USB-IK01, and ISE (Integrated Software Environment) of XILINX was used for the compiled program. ISE can be purchased from XILINX or an evaluation version can be downloaded from www.xilinx.com.

The figure below is a screen shot of ISE.

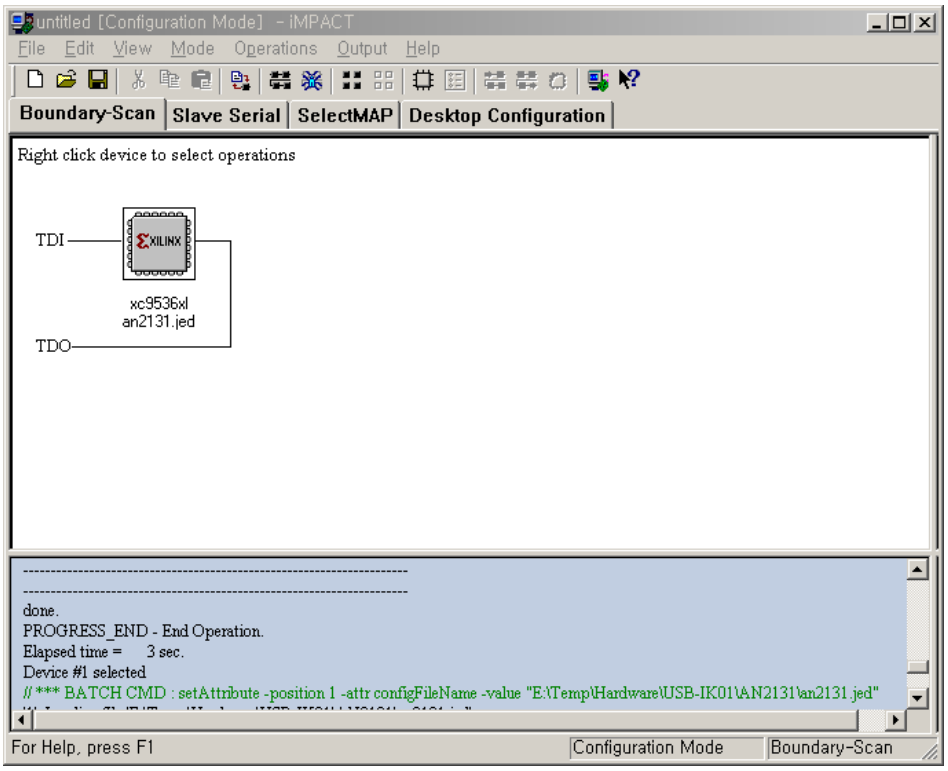


[Figure 4-2. ISE Execution Window]

For detailed program usage, please refer to the manual. The manual is installed together with the XILINX website or program installation.

4-3 Chip Program with using ISE

When VHDL compilation and implementation using ISE are finished, the JEDEC file is finally created. This file is recorded on the EPLD chip to perform the desired function. The figure below shows programming using the JTAG interface (Boundary Scan) (iMPACT is installed together when ISE is installed).



[Figure 4-3. iMPACT Execution Window]

For detailed program usage, please refer to the manual. The manual is installed together with the XILINX website or program installation.

5. Test

Connect the cables (RS232, USB) as shown in [Figure 4-1]. At this time, there is no need to connect the printer cable when EPLD program is not executed.

5-1 Ready To Test

If the communication program comm.exe is used for the test, the setting values are 38400bps, 8bit, No parity, 1 stop bit. First, set the DIP switch required for the test. The setting contents of the DIP switch are as shown in [Table 1.]. (Please refer to the VHDL source for details.)

(Note) Since the contents of EPLD can be modified by the user, the contents of the DIP switch below can be changed according to the user program.

[Table 1.]

Switch No	Description	Remark
1	It is connected to the input port (bit7) of PCF 8574, and when it is "ON", reading the input of 8574 reads '0'.	
2	When "ON", select 16-bit address serial EEPROM to read VID and PID from EEPROM. For 24LC64, it is a 16-bit address EEPROM. In case of "OFF", EZ-USB core recognizes that there is no serial EEPROM (except 24LC00)	
3	When "ON" as Memory Mode Bit0, it is '0'	
4	When "ON" with Memory Mode Bit1, it is '0'	

When MM is "00"

No external memory is used. That is, only the internal 8Kbyte RAM is used.

When MM is "01"

Uses only external RAM.

When MM is "10"

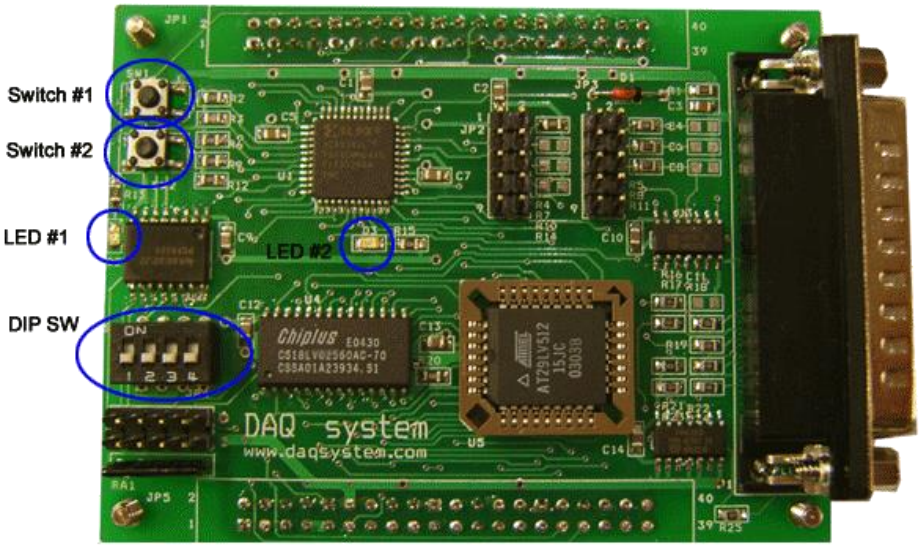
It uses external RAM and ROM. RAM address 0x0000, ROM address 0x8000

When MM is "11"

It uses external RAM and ROM.

EA (External Access) pin is '1', that is, the program is read from external ROM.

ROM address 0x0000, RAM address 0x8000



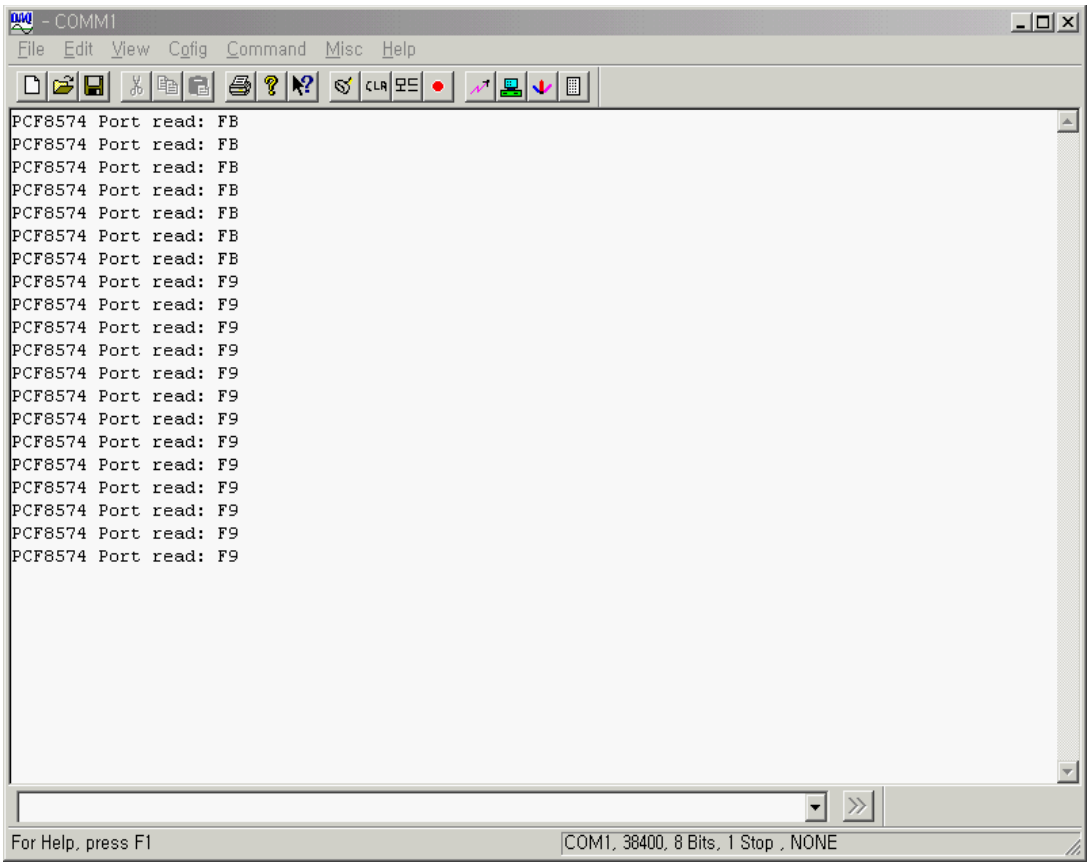
[Figure 5-1. USB-IK01 External Input/Output]

[If you look at Figure 5-1], you can check the input/output of the board to be used for the test. Also, please refer to Chapter 5 of "USB-EK01 User Manual" for the test method and program to use.

5-2 PCF8574 Test

The file used for the test can be found in the "Software₩Example₩USB-IK01₩PCF8574" folder of the CDROM, and download "pcf8574.hex" and test it. When executed, the input value of 8574 is periodically transmitted through the serial port. The transmitted contents can be checked using "COMM.exe".

If you press "Switch #2" here, the value changes. In [Figure 5-2], you can see that the value has changed from 0xFB to 0xF9.



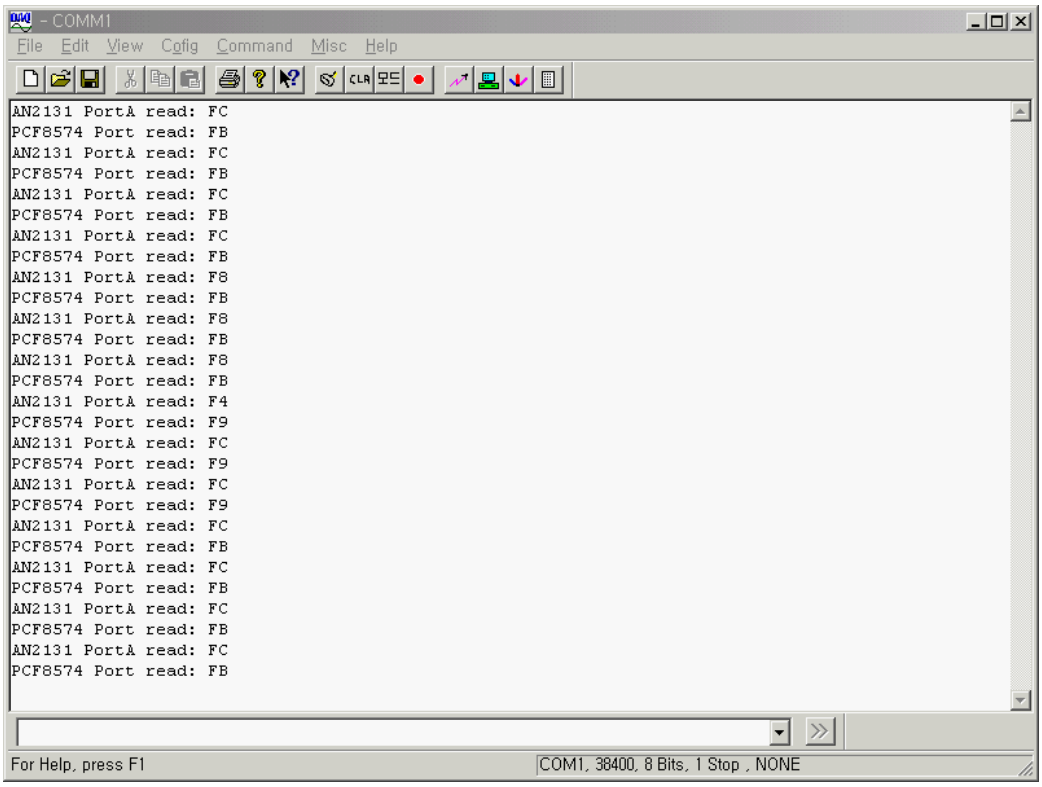
[Figure 5-2. PCF8574 Test window

5-3 EPLD Test

The file used for the test can be found in the "Software₩Example₩USB-IK01₩EPLD" folder of the CDROM, and download "epld.hex" and test it.

When executed, the values of PCF8574 and 8051 port A are periodically read and transmitted through the serial port. The transmitted contents can be checked by using "COMM.exe", and LED 1/2 lights up periodically. Here, if "Switch #1" or "Switch #2" is pressed, the input value is changed.

It can be confirmed by looking at [Figure 5-3].

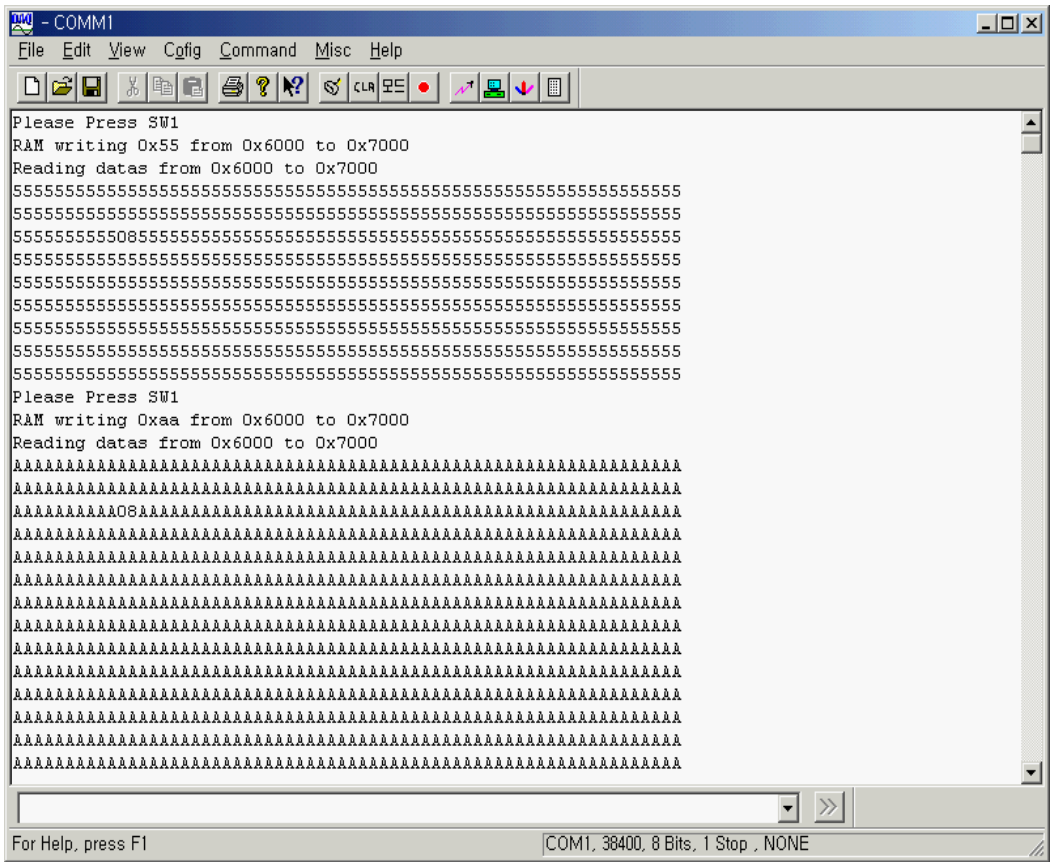


[Figure 5-3. EPLD Test window]

5-4 RAM Test

The file used for the test can be found in the "Software₩Example₩USB-IK01₩RAMTEST" folder of the CDROM, and download "ramtest.hex" and test it. When executed, it asks to press "Switch #1" through the serial port. When "Switch #1" is pressed, record and check the 0x55 value from RAM address 0x6000 to 0x7000. When "Switch #1" is pressed again next time, record and check the 0xAA value from RAM address 0x6000 to 0x7000.

The transmitted contents can be checked using "COMM.exe" as shown in [Figure 5-4].

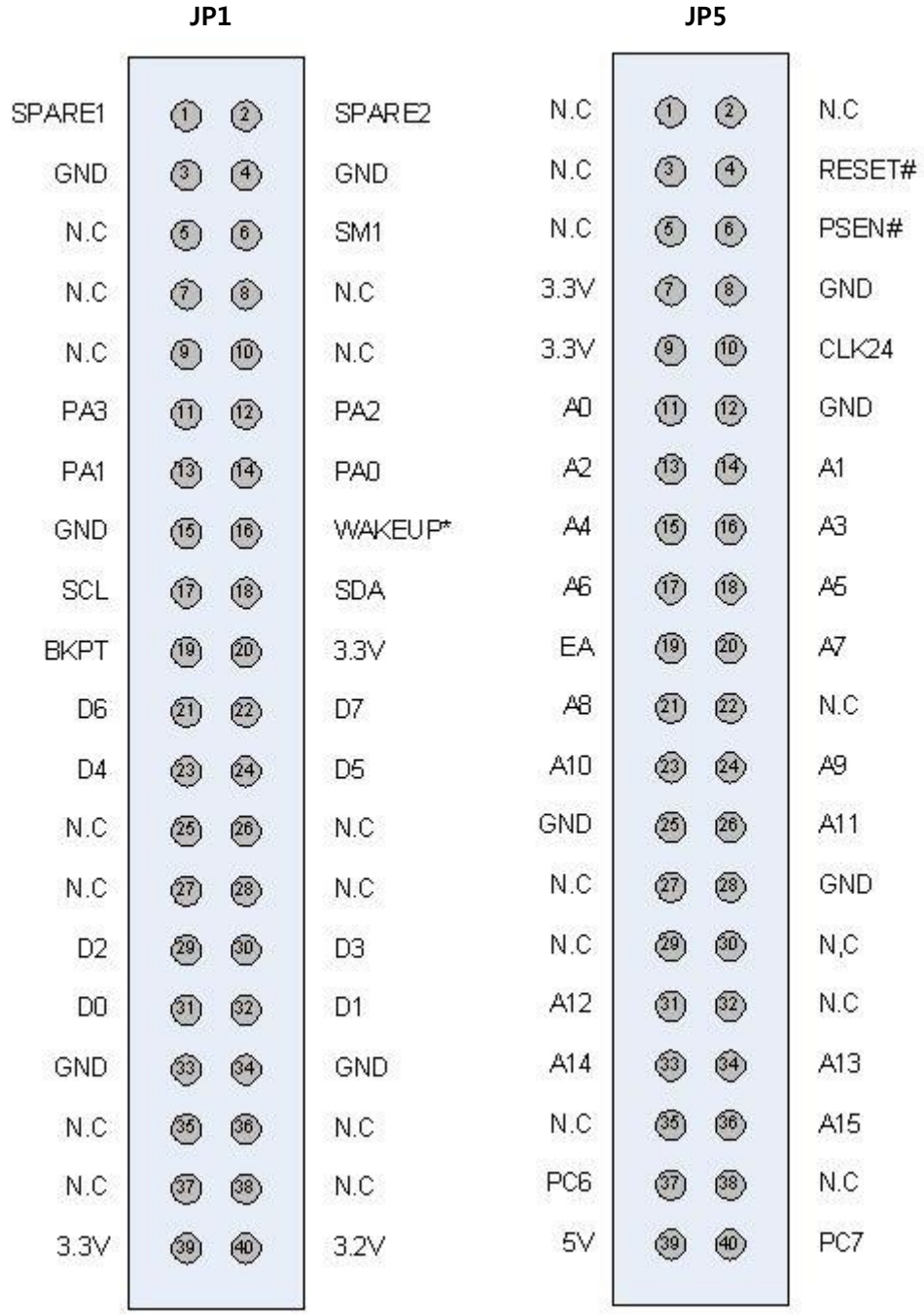


[Figure 5-4. RAM Test window]

Appendix

A-1 Connector (JP1 and JP5) PIN Map

The connectors on both sides of the USB-IK01 board can be connected to the USB-EK01. (see Section 3-3)



<JP1 Connector Pin Map>

PIN No.	Name	Description
1	SPARE1	EPLD Spare 1
2	SPARE2	EPLD Spare 2
3	GND	Signal Ground
4	GND	Signal Ground
5	N.C	No Connection
6	SM1	Serial ROM select 1 (short to ground for 24LC64)
7	N.C	No Connection
8	N.C	No Connection
9	N.C	No Connection
10	N.C	No Connection
11	PA3	8051 General Purpose PortA 3
12	PA2	8051 General Purpose PortA 2
13	PA1	8051 General Purpose PortA 1
14	PA0	8051 General Purpose PortA 0
15	GND	Signal Ground
16	WAKEUP#	Wakeup input from CPU suspend
17	SCL	I2C signal clock
18	SDA	I2C signal data
19	BKPT	Break Point Output
20	3.3V	3.3V Power Supply
21	D6	Data bus 6
22	D7	Data bus 7
23	D4	Data bus 4
24	D5	Data bus 5
25	N.C	No Connection
26	N.C	No Connection
27	N.C	No Connection
28	N.C	No Connection
29	D2	Data bus 2
30	D3	Data bus 3
31	D0	Data bus 0
32	D1	Data bus 1
33	GND	Signal Ground
34	GND	Signal Ground
35	N.C	No Connection
36	N.C	No Connection
37	N.C	No Connection
38	N.C	No Connection

39	3.3V	3.3V Power Supply
40	3.3V	3.3V Power Supply

<JP5 Connector Pin Map>

PIN No.	Name	Description
1	N.C	No Connection
2	N.C	No Connection
3	N.C	No Connection
4	RESET#	Reset Output (Low Active)
5	N.C	No Connection
6	PSEN#	Program strobe Enable
7	3.3V	3.3V Power Supply
8	GND	Signal Ground
9	3.3V	3.3V Power Supply
10	CLK24	CPU clock 24Mhz
11	A0	Address Bus 0
12	GND	Signal Ground
13	A2	Address Bus 2
14	A1	Address Bus 1
15	A4	Address Bus 4
16	A3	Address Bus 3
17	A6	Address Bus 6
18	A5	Address Bus 5
19	EA	External Access Input
20	A7	Address Bus 7
21	A8	Address Bus 8
22	N.C	No Connection
23	A10	Address Bus 10
24	A9	Address Bus 9
25	GND	Signal Ground
26	A11	Address Bus 11
27	N.C	No Connection
28	GND	Signal Ground
29	N.C	No Connection
30	N.C	No Connection
31	A12	Address Bus 12
32	PC3	8051 General Purpose PortC 3
33	A14	Address Bus 14
34	A13	Address Bus 13

35	N.C	No Connection
36	A15	Address Bus 15
37	PC6	8051 General Purpose PortC 6
38	N.C	No Connection
39	N.C	No Connection
40	PC7	8051 General Purpose PortC 7

A-2 Repair Regulations

Thank you for purchasing DAQ SYSTEM's product. Please refer to the following regarding Customer Service stipulated by DAQ SYSTEM.

(1) Please read the user's manual and follow the instructions before using the DAQ SYSTEM product.

(2) When returning the product to be repaired, please send it to the head office with the symptoms of the malfunction as well.

(3) All DAQ SYSTEM products have a one-year warranty.
-. The warranty period is counted from the date the product is shipped from DAQ SYSTEM.
-. Peripherals and third-party products not manufactured by DAQ SYSTEM are covered by the manufacturer's warranty.
-. If repair is required, please contact the contact points below.

(4) Even during the free repair warranty period, paid repairs are made in the following cases.
① Failure or damage caused by not following the user's manual
② Failure or damage caused by customer negligence during product transportation after purchase
③ Natural phenomena such as fire, earthquake, flood, lightning, pollution, etc. or power supply exceeding the recommended range malfunction or damage
④ Failures caused by inappropriate storage environment (eg, high temperature, high humidity, volatile chemicals, etc.) damaged
⑤ Failure or damage due to unreasonable repair or modification
⑥ Products whose serial number has been changed or intentionally removed
⑦ In the event that DAQ SYSTEM determines that it is the customer's negligence for other reasons

(5) The customer must bear the shipping cost of returning the repaired product to DAQ SYSTEM.

(6) The manufacturer is not responsible for any problems caused by incorrect use regardless of our Warranty provisions.

References

1. EZ-USB Manual Technical Reference Manual V1.10

-- Cypress Semiconductor Corporation

2. XC9500XL High-Performance CPLD Family Data Sheet

-- Xilinx Inc.

3. ISE Quick Start Tutorial

-- Xilinx Inc.

4. VHDL for PROGRAMMABLE LOGIC

-- KEVIN SKAHILL, (Addison Wesley)

MEMO

Contact Point

Web sit : https://www.daqsystem.com

Email : postmaster@daqsystem.com

DAQ SYSTEM
Measurement & Automation