MIPI-ADP01

User Manual

Version 1.0



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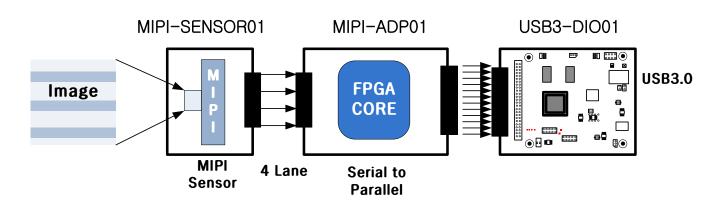
Contents

1.	M	IPI-ADP01	Introduction	2
2.	M	IIPI-ADP01	Function	8
2	2-1	J1 Connector		9
2	2-2	J3 Connector		10
2	2-3	J4 Connector		11
2	2-4	J5 Connector		12
2	2-5	SW1		13
Аp	pe	ndix		
,	۹-1	Board Size		14
/	۹-2	Repair Regula	tions	15

1. MIPI-ADP01 Introduction

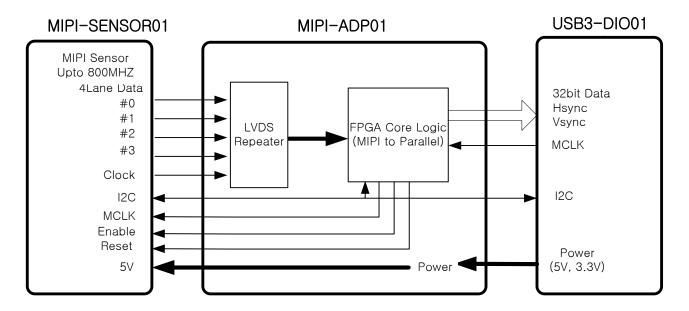
MIPI-ADP01 board is a function of transferring to the USB-DIO01 board after being converted into parallel signals received from the MIPI serial signal through MIPI-SENSOR01. The maximum transmission speed is about $600 \sim 700 \text{Mbps/Lane}$.





[Figure 1-1. MIP-ADP0101 Connection]

The block diagram of MIPI-ADP01 is in Figure 1-2. All functions are controlled by the FPGA, and also, the power received from USB3-DIO01 supply to MIPI sensor board.



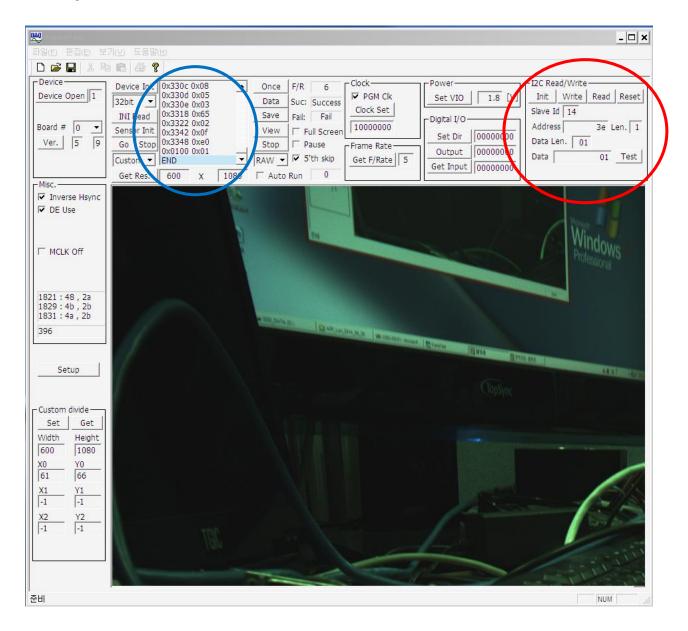
P.S) I2C : Sensor Setting or Lane Information (from USB3-DIO01 to MIPI sensor) MCLK : Variable Clock 1 \sim 68MHz

[Figure 1-2. MIPI-ADP01 Block Diagram]

The USB3-DIO01 can be communicated with the MIPI sensor through I2C as like [Figure 1-2]. Also, it can be controlled the FPGA of MIPI-ADP01 via I2C.

Some of the features of the I2C-related and USB3-DIO01 sensor INI files, they are as follows: This will be described with reference to the USB3-DIO01 sample program.

(We have been promoting integration of Input/Output function, so the sample program may be changed.)



The part of blue circle shows a value that MIPI sensor initialization file. It can be read in "INI read". This initialization file is different for each sensors, there are Slave ID and Address and Data between [REGISTER] and [END] command.

The initialization file will be read all at once at "INI read" button. You can be written an address and data one by one in part of red circle (I2C Read/Write part). In this case, sensor address should be used to a Slave ID. It is fixed to 0x3c.

Example 1) OV5640(5M).ini File Structure

```
[REGISTER]
Slave
       0x3C //change slave ID as Sensor
SLEEP
        100
0x3103 0x11
0x3008 0x82
0x3008 0x42
0x3103 0x03
0x3017 0x00
0x3018 0x00
0x3034 0x1a
0x3035 0x12
0x3036 0x69
0x3037 0x13
0x3108 0x01
0x3630 0x36
0x3631 0x0e
0x3632 0xe2
.....
0x501f 0x03
0x440e 0x00
0x4837 0x16
0x5000 0x06
0x5001 0x00
0x3a0f 0x36
0x3a10 0x2e
0x3a1b 0x38
0x3a1e 0x2c
0x3a11 0x70
0x3a1f 0x18
0x3008 0x02
[END]
```

When you want to control the FPGA of MIPI-ADP01, Slave Address will be fixed to 0x14. The MIPI control signals that you want have to be written the data to the corresponding address register.

Example 2) When the FPGA controls, SLAVE ADDRESS(7bit) is fixed to 0x14.

Register Address

0x1D: 0x03: MIPI 4 Lane 0x01: MIPI 2 Lane 0x00: MIPI 1 Lane

0x3D: It determines the GPIO In or Out direction.

"0" : Output "1" : Input

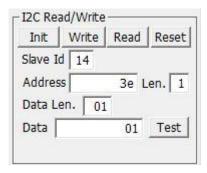
0x3E: S_RESET, ENB, CNT0,1,2,3 Control of J2 Connector (Refer to [Table 1])

bit0: S_RESET bit1: ENB bit4: CNT0 bit5: CNT1 bit6: CNT2 bit7: CNT3

0x3F : Read a bit on the set. (Read Only)
Reading order as bit7..bit0.

Note) The SLAVE ADDRESS should be represented 7bit in the above ***. Ini files.

For example, if slave address is 0x40, this value is 0x20 that shifted one bit to the right.



I2C Read / Write block is composed of a function associated with the transmission of the I2C.

(1) "Init" Button

It will initiate the resources for the I2C system.

(2) "Write" Button

Transmit the data through I2C for control to MIPI or CMOS camera.

(3) "Read" Button

Receive the data through I2C for control to MIPI or CMOS camera.

(4) "Reset" Button

There is Initialization resource of I2C system.

(5) "Slave ID ": Slave Address

"Reg. Addr ": Slave Register Address

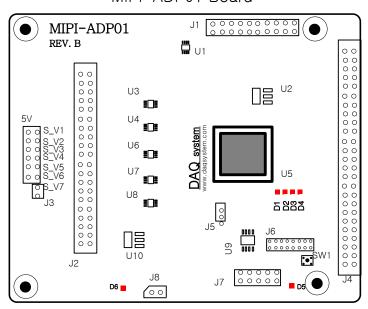
"Addr Len :" : Address Length

"Data Len:" : Data Length

"Data:": Data that will transmit

2. MIPI-ADP01 Function

MIPI-ADP01 names and functions of each are described below.



MIPI-ADP01 Board

No.	Name	Description	
1	U1	I2C (Low Voltage Level Translator)	
2	U2, U10, U16	1.3V, 2.5V, 3.3	
3	U3, U4, U6, U7, U8	Differential Translator/Repeater	
4	U5 FPGA		
5	U9	16Mbit, Flash memory	
6	J1, J6	For Test	
7	J2	MIPI Board Connection Connector (For MIPI signals)	
8	J3	Sensor Power Selection Jumper	
9	J4	USB3-DIO01 Connection Connector (For Parallel signals)	
10	J5	Control Signal (Voltage Level)	
11	J7	JTAG(Joint Test Action Group)	
12	18	External Power Connector (3.3V)	
13	SW1	3.3V Reset Switch	

- LED is also to check for internal operations.
- LED D1 turns on when vertical synchronization signal detects. (Vsync)
- LED D2 turns on when the horizontal synchronization signal detects. (Hsync).
- LED D3 shows a signal that divide into 24 parts of 50MHz clock.
- LED D4 shows a signal that divide into 4 parts of Vsync.
- LED D5 turns on when power is applied to the board and the initialization ends up.
- LED D6 turns on when power 3.3V is applied to the board.

2-1 J2 Connector

It is connected to the MIPI SENSOR board, signals are as follows.

J2



[Figure 2-1. J2 Connector (Top View)]

[Table 1. J2 Connector Description]

No.	Name	Description	Remark
1	SEN_VOUT1	User Defined Power	Connected S_V1 of J3
2	SEN_VOUT2	User Defined Power	Connected S_V2 of J3
3	SEN_VOUT3	User Defined Power	Connected S_V3 of J3
4	SEN_VOUT4	User Defined Power	Connected S_V4 of J3
5	GND	Ground	
6	GND	Ground	
7	SCL	Serial Clock	
8	DATAP_0	MIPI 1 Lane Positive	
9	SDA	Serial Data	
10	DATAN_0	MIPI 1 Lane Negative	
11	GND	Ground	
12	GND	Ground	
13	ENB	Enable	
14	DATAP_1	MIPI 2 Lane Positive	
15	S_RESET	Reset	
16	DATAN_1	MIPI 2 Lane Negative	
17	GND	Ground	
18	GND	Ground	
19	CNT0	Control 0	
20	DATAP_2	MIPI 3 Lane Positive	
21	CNT1	Control 1	
22	DATAN_2	MIPI 3 Lane Negative	
23	GND	Ground	
24	GND	Ground	
25	CNT2	Control 2	
26	DATAP_3	MIPI 4 Lane Positive	
27	CNT3	Control 3	

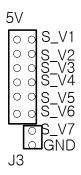
28	DATAN_3	MIPI 4 Lane Negative	
29	GND	Ground	
30	GND	Ground	
31	GND	Ground	
32	CLKP	MIPI Clock Positive	
33	GND	Ground	
34	CLKN	MIPI Clock Negative	
35	MCLK	Master Clock	
36	GND	Ground	
37	GND	Ground	
38	GND	Ground	
39	SEN_VOUT5	User Defined Power	Connected S_V5 of J3
40	SEN_VOUT6	User Defined Power	Connected S_V6 of J3

2-2 J3 Connector

The J3 connector is used to supply external power to the MIPI sensor. It is connected by a jumper and 5V line of the horizontal by default.

 S_V7 determines the level of SCL / SDA / S_RESET / CNT0~3 / MCLK signal line (1.8~3.3V) (Refer to J5 Connector)

Caution) It is prohibited more than 3.3V in case of S_V7.



[Figure 2-2. J3 Connector (Top View)]

2-3 J4 Connector

The following figure shows the external input and output board of J4 connector pin map. It is used to the Image Control Signals (Hsync, Vsync, Data Enable, Clock).

J4



[Figure 2-3. J4 Connector (Top View)]

[Table 2. J4 Connector Description]

No.	Name	Description	Remark
1	+3.3V	+3.3V Power	
2	+5V	+5V Power	
3	DIO_0	Digital Input/Output 0	
4	DIO_1	Digital Input/Output 1	
5	DIO_2	Digital Input/Output 2	
6	DIO_3	Digital Input/Output 3	
7	DIO_4	Digital Input/Output 4	
8	DIO_5	Digital Input/Output 5	
9	DIO_6	Digital Input/Output 6	
10	DIO_7	Digital Input/Output 7	
11	DIO_8	Digital Input/Output 8	
12	DIO_9	Digital Input/Output 9	
13	DIO_10	Digital Input/Output 10	
14	DIO_11	Digital Input/Output 11	
15	DIO_12	Digital Input/Output 12	
16	DIO_13	Digital Input/Output 13	
17	DIO_14	Digital Input/Output 14	
18	DIO_15	Digital Input/Output 15	
19	GND	Ground	
20	GND	Ground	
21	DIO_16	Digital Input/Output 16	
22	DIO_17	Digital Input/Output 17	
23	DIO_18	Digital Input/Output 18	
24	DIO_19	Digital Input/Output 19	
25	DIO_20	Digital Input/Output 20	
26	DIO_21	Digital Input/Output 21	

27	DIO_22	Digital Input/Output 22	
28	DIO_23	Digital Input/Output 23	
29	DIO_24	Digital Input/Output 24	
30	DIO_25	Digital Input/Output 25	
31	DIO_26	Digital Input/Output 26	
32	DIO_27	Digital Input/Output 27	
33	DIO_28	Digital Input/Output 28	
34	DIO_29	Digital Input/Output 29	
35	DIO_30	Digital Input/Output 30	
36	DIO_31	Digital Input/Output 31	
37	DIO_32	Digital Input/Output 32	PCLK(Pixel Clock)
38	DIO_33	Digital Input/Output 33	Vsync
39	DIO_34	Digital Input/Output 34	Hsync
40	DIO_35	Digital Input/Output 35	DE(Data Enable)
41	DIO_36	Digital Input/Output 36	
42	DIO_37	Digital Input/Output 37	
43	DIO_38	Digital Input/Output 38	
44	DIO_39	Digital Input/Output 39	
45	REV1	Reserver 1	nReset
46	U_SDA	Serial Data	SDA
47	REV0	Reserved 0	MCLK(Master Clock)
48	U_SCL	Serail Clock	SCL
49	GND	Ground	
50	GND	Ground	

2-4 J5 Connector

The signal output from the FPGA (SCL, SDA, MCLK, S_RESET, ENB, CNT0 .. 3) can be determined the voltage level.

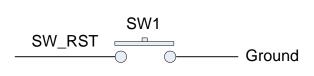
The default connection is 2.5V [2..3 Connection]. When connecting [1..2], output to the voltage that is determined to user.(prohibited more than 3.3V)



[Figure 2-4. J5 Connector (Top View)]

2-5 SW1

It is 3.3V Power Reset Switch (Low Active).

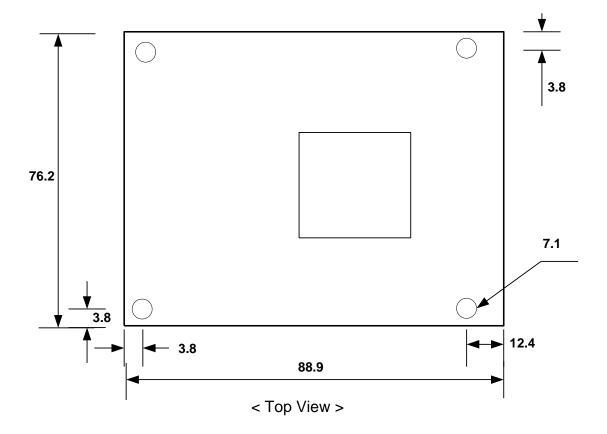


[Figure 2-5. SW1 switch]

Appendix

A-1 Board Size

The external sizes of the board are as follows.



A-2 Repair Regulations

Thank you for purchasing a DAQSYSTEM product. Please refer to the following regarding Customer Service regulated by DAQSYSTEM.

- (1) Read the user manual and follow the instructions before using the DAQSYSTEM product.
- (2) When returning the product to be repaired, please write down the symptoms of the failure and send it to the head office.
- (3) All DAQSYSTEM products have a 1-year warranty.
 - -. Warranty period counts from the date the product is shipped from DAQSYSTEM.
 - -. Peripherals and third-party products not manufactured by DAQSYSTEM are covered by the manufacturer's warranty..
 - -. If you need repairs, please contact the Contact Point below..
- (4) Even during the warranty period, repairs are charged in the following cases..
 - 1) Failure or damage caused by use without following the user's manual
 - ② Failure or damage caused by customer's negligence during product transportation after purchase
 - 3 Failure or damage caused by natural phenomena such as fire, earthquake, flood, lightning, pollution, or power supply exceeding the recommended range
 - 4 Failure or damage caused by inappropriate storage environment (e.g. high temperature, high humidity, volatile chemicals, etc.)
 - ⑤ Breakdown or damage due to unreasonable repair or modification
 - 6 Products whose serial number has been changed or removed intentionally
 - 7 If DAQSYSTEM determines that it is the customer's fault for other reasons
- (5) Shipping costs for returning the repaired product to DAQSYSTEM are the responsibility of the customer.
- (6) The manufacturer is not responsible for any problems caused by misuse, regardless of our warranty terms.

MEMO

Contact Point

Web sit : https://www.daqsystem.com

Email: postmaster@daqsystem.com

